9950-450

DOE/JPL 954854 - 80/8
Distribution Category UC-63

PHASE 2 OF THE ARRAY AUTOMATED ASSEMBLY TASK

FOR THE LOW COST SILICON SOLAR ARRAY PROJECT

(NASA-CR-163805) PHASE 2 OF THE ARRAY AUTOMATED ASSEMBLY TASK FOR THE LOW COST SILICON SOLAR ARRAY PROJECT Final Report (Solarex Corp., Rockville, Md.) 107 p HC A06/MF A01 CSCL 10A G3/44

N81-12552

Unclas 29410

FINAL REPORT

NOVEMBER 1980

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"The JPL low-cost Silicon Solar Array Project is sponsored by the U.S. Department of Energy and forms part of the solar Photovoltaic Conversion Program to initiate a major effort toward the development of low-cost solar arrays. This work was performed for the Jet Propulsion Laboratory, California Institute of Technology by agreement between NASA and DOE."

SUMMARY

Studies were conducted on several fundamental aspects of electroless nickel/solder metallization for silicon solar cells. A process proposed by Motorola, which precedes the electroless nickel plating with several steps of palladium plating and heat treatment, was compared directly with single step electroless nickel plating.

Work was directed toward answering specific questions concerning the effect of silicon surface oxide on nickel plating, effects of thermal stresses on the metallization, sintering of nickel plated on silicon, and effects of exposure to the plating solution on solar cell characteristics. The Motorola process was compared with simple electroless nickel plating in a series of parallel experiments.

It was demonstrated by ellipsometry measurements that the electroless nickel plating solution dissolves silicon dioxide. Measurements of tab pull strengths and electrical characteristics of cells show that the presence of the oxide has no effect on cell properties. Removal of the oxide by the plating solution obviously does require some time, but the delay in onset of nickel plating caused by the presence of a normal atmospheric oxide on silicon is very short.

It was also shown, by sheet resistance measurments and gravimetric measurements, that the plating solution dissolves some silicon before depositing nickel. This phenomenon dictates that special care be taken during the diffusion process to assure that the p-n junction is deep enough to survive the silicon dissolution.

Brief sintering at relatively low temperatures after nickel plating sometimes increases otherwise poor adhesion. It has been shown by leakage current and electron microprobe measurements that sintering can safely be conducted for long times at 300°C, but it has also been shown that excellent adhesion can be obtained without sintering.

Cells with electroless nickel/solder metallization have been shown to survive perfectly for over 1,000 hours under bias-temperature-humidity stresses of 0.45 volt forward bias at 95°C and 85% relative humidity. This metallization also survives 763 hours at 100°C and 25 cycles of thermal shock from -40°C to +100°C, while temperature extremes of -65°C and +150°C are too severe.

The Motorola process was found to be extremely lengthy and cumbersome, and was also found to produce a product virtually identical to that produced by single step electroless nickel plating, as shown by adhesion tests and electrical characteristics of cells under illumination.

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1. INTRODUCTION

The program described in this report is a supplement to an earlier process program. It focuses attention on one key step of a proposed process sequence for mass production of inexpensive silicon solar arrays for terrestrial use. The process step of concern is the metallization of the solar cell, and the specific method of interest involves electroless nickel plating followed by solder dipping.

Solarex has proposed that the metallization be accomplished by a single electroless plating of nickel followed by a dip in molten solder, and Solarex manufactures solar cells using this procedure. Motorola has recommended a process which includes the electroless nickel plate and solder dip of the Solarex process, but which precedes these steps with a number of additional steps of palladium plating, cleaning and annealing. Motorola has claimed that these additional steps are necessary to assure proper ohmic contact with the silicon while at the same time avoiding excessive nickel penetration into the silicon.

This program comprises a technical comparison of the Solarex and Motorola processes, and at the same time it incorporates studies of some of the underlying processes which are important to the understanding and controlling of

the total plating process. The work includes five experimental tasks: the first four of these tasks are studies of some physical processes which are fundamental to the overall metallization process, while the fifth task is an assessment of the Motorola process through a direct experimental comparison of the Motorola process with a single step electroless nickel plating process like that used by Solarex.

Work has been completed on all five of these assigned tasks.

1.1 Effects of Surface Oxide Thickness and Sintering Temperature

Surface oxides on silicon solar cells are recognized as a potential source of difficulty in applying contact metallization to the cells. Fabrication processes include etching and cleaning procedures designed to remove surface oxides from the silicon, but these procedures are not perfect, and some oxide, of undetermined and perhaps variable thickness, will usually be carried over to the metallization step. This oxide may be the cause of poor adhesion, poor ohmic contact, or both, and may lead to poor reproducibility in the metallization process.

Cells are sometimes heated after the metallization step, sometimes at high temperatures, sometimes at relatively low temperatures, in an effort to improve the adhesion and electrical contact properties, presumably through diffusion of the contact metal through the oxide and into the silicon.

The first experimental task in this program is an assessment of the influences of silicon surface oxide thickness and sintering temperature on the adhesion and electrical characteristics of electroless nickel plates on oxidized silicon.

1.2 Environmental Testing of Electroless Nickel Contacts

The Solarex metallization process under study here employs an electroless nickel plating followed by a dip in molten solder. The quality of the bond produced depends upon the quality and cleanliness of the silicon surface being plated, upon the quality of the electroless nickel plate itself, and upon the effectiveness of any sintering action.

The bond produced by this process appears adequate for many solar cell applications, but it may be weaker than bonds formed by some other metallization processes. While

the initial construction generally exhibits perfectly adequate properties, there is some concern as to whether it will perform adequately over an extended period of cell operation under a variety of adverse environmental conditions.

The second experimental task of the program is a study of the integrity of the silicon - metal bond during environmental stress tests. No accelerated stress regimen has yet been demonstrated to be a reliable or useful predictor of solar cell lifetime behavior, but four relatively demanding stress tests have been selected which might be predicted to have some deleterious effect on the silicon - metal bond.

Electrical characteristics of the cells are compared before and after the stresses, and pull tests are conducted on the cells after stress and also on a group of control cells.

1.3 Nickel Penetration of Silicon

Metallized solar cells are usually heated, under conditions ranging from mild to severe, to improve the contact between the silicon and the metallization. A critical concern in the case of nickel metallization is

the possibility of nickel diffusion at elevated temperatures through the front junction of the solar cell, an occurrence which would create paths of high current leakage and could effectively destroy the solar cell.

This task is a study of nickel penetration into silicon as a function of sintering temperature and time in a range that might be experienced in solar cell manufacture. Detection of nickel diffusion has been accomplished by microprobe analysis.

1.4 Effect of Nickel Plating Solution on Solar Cells

This task comprises measurements of electrical characteristics of cells fabricated using a range of nickel plating times in an effort to detect any detrimental effects to the p-n junction of the solar cell which might be caused by exposure to the plating solution.

1.5 Evaluation of Motorola Plating Process

The final experimental task is the evaluation of the Motorola plating process relative to simple electroless nickel plating.

The Motorola metallization process (1) has been considered by Motorola "to contain the maximum number of process steps required for assured metallization of n-on-p solar cells with n+ front surfaces and p+ back surfaces." (2) Motorola has also cautioned, however, that the "process sequence reported here may require minor modifications to account for different types of solar cell substrates and to account for the previous processing history of substrates prior to metallization."

The Motorola process is a complex and lengthy one, culminating in an electroless nickel plating step. It is our purpose to devise and to perform experiments which will reveal any advantages which the complex Motorola process might provide over a single step electroless nickel plating, and to provide an overall assessment of the utility of the process.

2. SURFACE OXIDE THICKNESS AND SINTERING TEMPERATURE

A large number of diffused silicon wafers (phosphine diffusion on P type 100 Cz wafers) were oxidized using a variety of techniques, including heating in air, heating in steam and heating in oxygen. Oxide thicknesses were measured using ellipsometry.

Heating in an oxygen atmosphere proved to be the best method for obtaining uniformity and reproducibility of oxide thicknesses; uniformity of oxide thickness on any single wafer or within a single batch of wafers was extremely good, with variations greater than two or three Angstroms being unusual.

Initial efforts at plating nickel and sintering gave quite variable and confusing results, and eventually led us to believe that the electroless nickel plating solution was dissolving the silicon oxide films before depositing nickel, a very interesting and significant conclusion.

2.1 Dissolution of Silicon Oxide Films

We have conducted a series of experiments, again using ellipsometry to measure oxide film thicknesses, to determine conclusively whether or not the oxide film is being dissolved by the plating solution.

In the first of these experiments, a group of three silicon wafers with different oxide thicknesses were immersed in our electroless nickel plating solution at 90°C for 12 min, at the end of which time no nickel had plated on them. Oxide thicknesses were measured again and the wafers were immersed in the plating solution for 6 min more. Nickel plated on two of the wafers, and the oxide thickness was measured on the third one. This experiment is summarized in Table 1.

Table 1

Oxide Dissolution by Nickel Plating Solution

Operation	Results		
	Cell D	Cell E	Cell H
Measure oxide thickness	110 Å	157 Å	177 Å
Immerse 12 minutes	No Plate	No Plate	No Plate
Measure oxide thickness	55 Å	92 Å	114 Å
Immerse 6 minutes	Plated	Plated	No Plate
Measure oxide thickness	----	----	51 Å

In a second experiment, a standard electroless nickel plating bath (2,3) was used at 90°C without the nickel chloride. This bath contained 100 g ammonium chloride, 20 g sodium hypophosphite, 168 g sodium citrate, 250 ml conc ammonium hydroxide, and 1750 ml deionized water. Two cells were immersed in the bath for intervals of three

minutes and oxide film thicknesses were measured after each interval. Data are shown in Table 2.

Table 2

Oxide Dissolution Without $NiCl_2$

Time	Oxide Film Thickness	
	Cell E3	Cell H4
Before immersion	157 Å	177 Å
After 3 minutes immersion	108 Å	135 Å
After 6 minutes immersion	69 Å	82 Å
After 9 minutes immersion	Dark blotches (blue to golden brown) stained both cells.	

In a third experiment, a solution was used which was the same as that used in the second experiment except that the sodium citrate was initially eliminated and was added at a later point in the experiment. Results of this experiment are outlined in Table 3. The control wafer had no diffusion and no added oxide.

In this third experiment, extra NH_4OH was added before adding sodium citrate, because silicon dioxide is known to dissolve in strongly alkaline solutions, but the NH_4OH had no measurable effect.

Table 3

Oxide Dissolution Without $NiCl_2$
Initially No Sodium Citrate

Operation	Results (Oxide Thicknesses) Cell H3	Cell E2	Control
Measure oxide thickness	177 Å	155 Å	---
Immerse 3 min, measure oxide	157 Å	131 Å	Blue-brown stain
Immerse 9 min, measure oxide	157 Å	133 Å	
Add 250 ml conc NH_4OH Immerse 3 min, measure oxide	157 Å	133 Å	
Add 168 g sodium citrate Immerse 3 min, measure oxide	152 Å	114 Å	
Immerse 6 min, measure oxide	71 Å	37 Å	
Immerse 3 min	Blue-brown stain on both cells		

Obviously the electroless nickel plating solution dissolves the oxide film from the silicon and nickel begins to plate only after the oxide thickness has been reduced to some fairly low level (about 50 Å or less). It is also clear that the plating solution minus the nickel salt dissolves the oxide, but that when both the nickel salt and the sodium citrate are left out the solution dissolves only a small amount of oxide before the dissolution stops completely.

The blue-brown stain is formed even in the absence of the nickel salt and the citrate. We do not know the identity of the stain, but the best guess would be that it is a lower

oxide of silicon or perhaps an oxyphosphorus silicon compound. We have observed this stain on cells from which nickel has peeled and also on cells where the nickel - silicon adhesion has appeared to be very good, and we do not know that it is harmful in any way.

Now that we know the plating solution dissolves the silicon oxide down to a thickness of about 50 Å or less before plating any nickel, this task is resolved to a comparison of silicon containing an oxide film of 50 Å or thicker with silicon from which the oxide has been stripped as completely as possible.

2.2 Nickel Plating

A number of diffused wafers were plated with nickel, some with oxide films and some without. All wafers were cleaned with HF (about 2.5%) to remove oxide, and about 70 Å of oxide was grown thermally in O_2 on approximately one-third of the specimens. A pattern of buses, each about 1.5 mm wide, was formed on the wafers using Kapton tape. The oxidized wafers were plated for 10 min at 90°C in the electroless nickel bath, while half of the unoxidized wafers were plated for 10 min and half for 6 min. The thickness of the nickel plate on the oxidized specimens was expected to be less than the thickness of a 10 min plate

but greater than the thickness of a 6 min plate on unoxidized silicon.

2.3 Sintering

After plating, the Kapton tape was removed and specimens were sintered for 1 min on a hot plate at temperatures from 200°C to 300°C. Some specimens from each batch were not sintered. Temperatures above 300°C were not used because of our earlier observation of spontaneous nickel peeling from wafers sintered at 350°C or above. (4,5)

After sintering, the specimens were dipped in molten solder and tinned copper tabs, 1.75 mm wide, were soldered to the buses.

2.4 Tab Pull Tests

The complete fabrication process outlined in 2.2 and 2.3 was run on two batches of wafers, at two different times, and 90° tab pull tests were conducted on all of the tabs. The combined data are shown in Table 4.

The stains described in 2.1 were seen on a few wafers after pulling the tabs, but they appeared on both oxidized and unoxidized wafers.

Table 4

Tab Pull Data on Oxidized Silicon

Sinter Temp	Average Pull Strength (g) 70 Å Oxide 10 min plate	No Oxide 10 min plate	No Oxide 6 min plate
None	549	801	358
200°C	536	683	727
250°C	731	490	853
300°C	593	519	756

It appears clearly that the presence of oxide on the silicon surface prior to plating has no substantial effect on the contact adhesion.

It also appears that sintering has no useful effect, with the possible exception of the 6 min plate case, though even in this case the difference may not be significant because data scatter is always fairly large in this kind of experiment.

We are well aware that sintering, even as little as 30 sec at 200°C, can frequently bring about a great increase in adhesion in contacts which adhere only weakly without sintering, but the data of Table 4 demonstrate that excellent adhesion can be obtained without sintering (beyond a few seconds in molten solder).

2.5 Cells with Oxide Films

Oxide films were formed on a group of fifty (2¼" round) cells by heating in air at 450°C prior to nickel plating. Measurements of oxide thicknesses by ellipsometry ranged from 35 to 80 Angstroms. The oxide was removed by treatment with buffered HF from twenty-five of these cells, and all fifty cells were then nickel plated and solder dipped. Light I-V curves were determined at AM1 for several cells selected at random from each group, and tabs were soldered to and pulled from several cells in each group. Data are shown in Table 5.

Table 5

Oxide Effect on Cells

		Electrical Characteristics			Tab Pull Strength (g)
Set A Oxide removed		V_{oc}(mV)	I_{sc}(mA)	P_m(mW)	
	High	580	774	280	1531
	Low	542	652	233	28
	Mean	551	740	253	765
	S.D.	11	34	14	425
Set B Oxide - no HF					
	High	585	784	290	1644
	Low	546	738	273	113
	Mean	558	763	280	794
	S.D.	14	16	7	340

Electrical Measurements: Set A, 11 cells; Set B, 6 cells.

Tab Pull Data: Set A, 18 tabs; Set B, 24 tabs.

S.D. = Standard Deviation.

The cells which contained oxide appear slightly better in all characteristics, but the differences are not large relative to the standard deviations and there is no basis for suggesting that any real difference exists between the two groups.

This observation is exactly what would be predicted for the case where the plating solution dissolves silicon dioxide before depositing nickel.

3. ENVIRONMENTAL TESTING OF ELECTROLESS NICKEL CONTACTS

Four environmental stress tests have been selected to test the integrity of the silicon - nickel bond produced by the electroless nickel plating process. The tests include thermal cycle and thermal shock stresses as well as a 1,000 hour test at 150°C and a 1,000 hour bias - temperature - humidity test.

3.1 Cells

Solar cells have been constructed for the stress tests using the Solarex process in which nickel is plated directly on the silicon cell by the electroless plating method, with the cell then being dipped in molten solder. The cells are 2 cm squares cut from larger wafers and have a bus, about 1 mm wide, parallel to and close to one edge. Silicon used was Monsanto CZ 100, P type, ron dopant, 1-25 ohm-cm.

3.2 Tab Soldering

A procedure for soldering tinned copper tabs (70 mils wide, 2 mils thick) across the bus has been developed which uses minimum temperature and time in order to avoid

influencing the silicon - nickel interface. This soldering procedure is detailed in Appendix A. Electrical measurements made on representative samples before and after soldering showed no change, indicating that the tab bonding procedure was not substantially affecting the Si - Ni bond.

3.3 Cell Preparation for Stress Tests

On most of the cells, two tabs were soldered to the front bus, thus providing two data points from each cell. Area of the bond to the front bus could be reproduced within reasonably narrow limits, while bonds made to the back solder varied somewhat in area. It was also more convenient to measure electrical characteristics with no tab on the back.

The cells to be used for the bias - temperature - humidity (B-T-H) test required electrical connections to the backs, so a group of thirty cells had one tab soldered to the front bus and one near the back center. These cells are pictured in Figure 1.

3.4 Electrical Characteristics of the Cells

Electrical characteristics of the cells were measured before and after the stress tests. Current - voltage curves

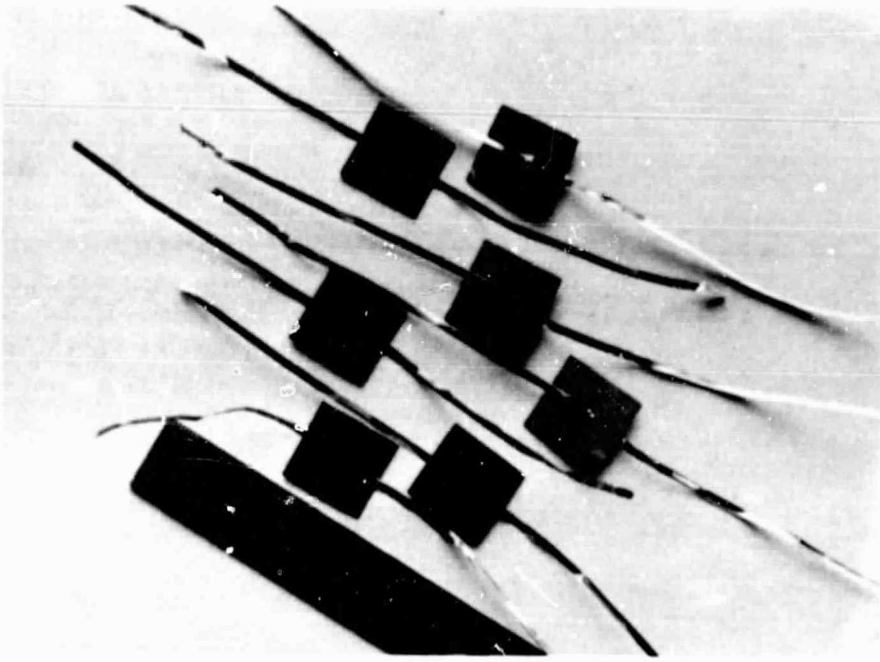

Figure 1 Bias - Temperature - Humidity Test Cells

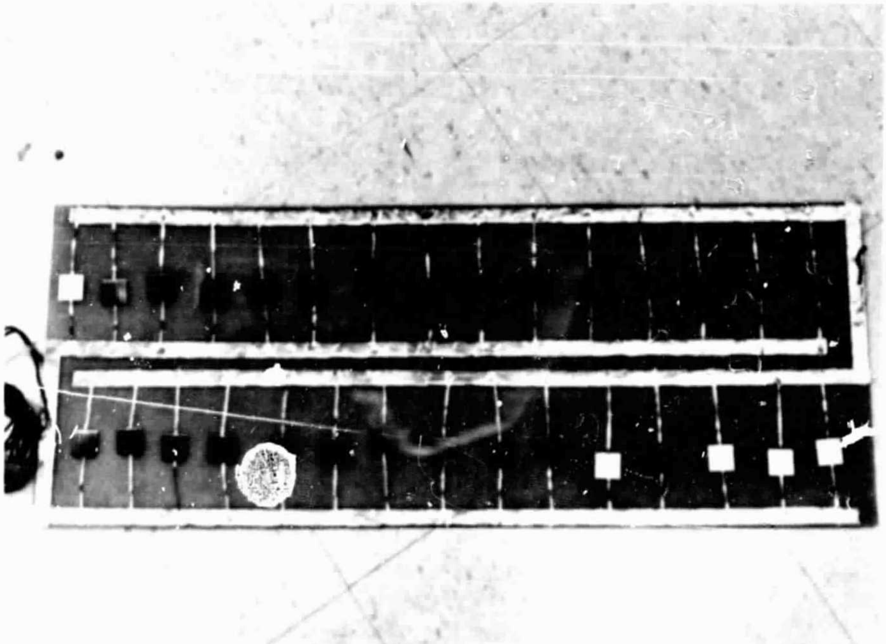

Figure 2 B- T- H Test Cell Array

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were recorded at AMO for full sun and with red and blue filters using a solar simulator for illumination. Calibration of the equipment was checked periodically with a standard cell.

Open circuit voltage (V_{oc}), short circuit current (I_{sc}), maximum power (P_m) and series resistance (R_s) were obtained from the current - voltage curves. In addition to these parameters, shunt resistance (R_{sh}) was also determined. This was done by measuring dark leakage current across the cell under reverse bias of 1.000 volt. The shunt resistance is then the ratio of the bias potential to the leakage current.

Series resistance could be a significant parameter in assessing the quality of the electrical contact between the silicon and the nickel, while shunt resistance should provide a direct indication of any junction penetration by nickel. The other electrical parameters are influenced in a less direct manner by these factors.

3.5 Stress Tests

3.51 Bias - Temperature - Humidity Test

Thirty cells for the B-T-H test were mounted by

soldering to a printed circuit board, after a suitable pattern had been etched in the copper conductor of the board and the remaining copper had been tinned with solder. The assembly, pictured in Figure 2, was then placed in a temperature - humidity chamber at 85°C and 85% relative humidity, and the cells, connected in parallel, were biased at 0.45 volt in the forward direction. This stress was continued for 1,074 hours.

The temperature - humidity chamber is a Blue M Electric Co. Model FR-256PBX equipped with temperature and humidity sensing, regulating and recording devices. The regulated biasing power supply was a Model 2015-R from Power Designs, Inc.

3.52 High Temperature Test

For the high temperature stress test, a group of thirty cells was placed in a thermally regulated oven at 150°C in air, and was left there for 1,008 hours. The oven was a Wylie Temperature Test Chamber Model C106-640.

3.53 Thermal Shock Test

For the thermal shock stress test, the high temperature bath was a stainless steel beaker of about 3.75

l capacity containing 2 l of fluorocarbon FC-40. It was heated on a hot plate whose heating rate was adjusted such that the liquid temperature (measured by an ordinary mercury bulb thermometer) would increase slowly at 150°C.

The low temperature bath was a stainless steel beaker of about 1.25 l capacity containing about 0.8 l of fluorocarbon FC-77. This beaker was immersed in a mixture of dry ice and iso-propyl alcohol in a larger stainless steel container of about 7.5 l capacity. The larger container was insulated by one inch of polyurethane foam. Temperature was measured by a thermocouple.

The cells under test were held in a small Teflon cassette with a capacity of 24 cells. The cassette containing the cells was placed in the high temperature bath with the temperature near 155°C, held there for five minutes, transferred to the low temperature bath, whose temperature was near -70°C, left for five minutes, then transferred again to the high temperature bath. This procedure was continued for 25 cycles, and two sets of cells were run to achieve a total of 29 cells. Transfer time was typically 4-6 seconds. Measured temperature of the cold bath typically rose about four degrees when the hot cassette was introduced

to the cold bath, while temperature variation in the hot bath was smaller than this when the cold cassette was introduced into it.

3.54 Thermal Cycle Test

A group of thirty cells was subjected to a thermal cycling stress in which they were first placed in a chamber at low temperature (-65 to -70°C) for ten minutes and then in a chamber at high temperature (150 to 155°C) for ten minutes, after which the cycle was repeated for a total of 100 cycles. Cells were contained in a Teflon cassette, and transfer time was less than 15 seconds.

The high temperature chamber was a Blue M Electric Company oven Model SW-17TA, and the low temperature chamber was a Wylie Temperature Test Chamber Model C106-640 using chilled nitrogen as the coolant.

3.55 Control Cells

Cells for a control group were stored in a cabinet at room temperature with a nitrogen atmosphere.

3.6 Results of Environmental Stress Tests

3.61 Results of Bias - Temperature - Humidity Test

A group of thirty cells was subjected to 85% relative humidity at 85°C under forward bias of 0.45 volt for 1,074 hours. At the end of the test these cells were unchanged in appearance, showing no visible evidence of corrosion or of contact deterioration.

Electrical characteristics, shown in Table 6, changed only slightly, with average V_{OC} increasing by 1.4%, I_{sc} decreasing by 0.7%, P_m increasing by 0.9%, R_s decreasing by 11.2% and R_{sh} increasing by about 30%. With the exception of the small decrease in short circuit current, all of these changes are in desirable directions. The relatively large increase in shunt resistance may be a result of elimination by oxidation of microscopic metallic shunts at cell edges.

Tab pull strengths after the stress, shown in Table 7, averaged 257 grams on the front (bus) tabs and 474 grams on the back solder tabs, with four failures at the tab joint and the remaining 56 failures occurring at the metal-silicon interface. No silicon damage was apparent in any instance. Tab pull strengths on the control cells averaged 177 grams.

Table 6

Electrical Characteristics of B-T-H Test Cells

Cell	V_{oc} (mV)	I_{sc} (mA)	P_m (mW)	R_s (ohm)	R_{sh} (ohms)
11	563(563)	137(130)	53.0(51.5)	.315(.320)	194(228)
12	560(562)	139(139)	55.0(55.0)	.348(.341)	131(168)
13	569(579)	140(138)	56.5(55.5)	.353(.453)	1159(1522)
14	537(545)	135(131)	50.5(51.0)	.328(.290)	132(204)
15	541(553)	135(139)	54.5(56.5)	.319(.313)	840(1075)
16	532(535)	133(131)	49.5(49.5)	.315(.283)	122(141)
17	534(544)	133(135)	52.0(54.0)	.331(.299)	286(357)
18	572(580)	142(140)	56.0(56.0)	.340(.302)	173(243)
19	569(576)	138(135)	54.5(54.5)	.400(.434)	309(394)
20	565(572)	140(138)	54.0(54.0)	.357(.327)	478(565)
21	532(541)	135(130)	53.0(54.0)	.381(.315)	6667(6410)
22	565(573)	139(138)	56.5(57.5)	.333(.295)	980(1647)
23	545(552)	138(136)	51.0(52.0)	.398(.350)	265(344)
24	575(579)	140(136)	58.0(56.0)	.414(.387)	1250(1901)
25	566(566)	143(140)	54.5(55.0)	.385(.304)	193(260)
26	530(539)	134(136)	52.0(53.5)	.322(.291)	980(1328)
27	569(580)	138(137)	54.5(55.0)	.392(.310)	193(226)
28	577(580)	138(142)	57.0(58.5)	.304(.299)	403(552)
30	530(538)	136(136)	52.0(53.0)	.381(.335)	1887(2212)
31	560(571)	134(135)	54.0(55.5)	.255(.204)	333(348)
32	530(540)	135(134)	51.5(52.5)	.351(.242)	980(1274)
35	560(572)	132(130)	51.0(53.5)	.416(.240)	3571(3984)
36	571(577)	135(127)	54.0(52.0)	.350(.298)	124(161)
37	566(580)	138(142)	56.0(58.5)	.320(.300)	1299(1841)
38	556(561)	137(137)	50.5(52.0)	.439(.361)	1515(1318)
39	569(580)	133(133)	53.0(54.0)	.391(.312)	187(240)
40	559(573)	133(135)	52.0(54.0)	.413(.381)	585(725)
43	560(568)	135(136)	56.0(57.0)	.336(.279)	352(571)
44	567(575)	126(123)	52.0(51.5)	.365(.298)	735(826)
45	555(557)	136(133)	56.0(54.5)	.324(.317)	233(3356)
Mean	556.1 (563.7)	136.2 (135.1)	53.7 (54.2)	.356 (.316)	885 (1147)
S.D.	15.5 (15.4)	3.4 (4.3)	2.2 (2.2)	.041 (.051)	1310 (1377)

Data before and (after) 1,074 hours at 85°C and 85% relative humidity biased at 0.45 volt in the forward direction.

Table 7

B-T-H Stress Tab Pull Strengths

	Pull Strength (g)			Pull Strength (g)	
Cell	Front	Back	Cell	Front	Back
11	573	488	26	179	420
12	0	417	27	332	71
13	198	539	28	184*	590
14	99	227	30	454*	516
15	335	252	31	113	505
16	0	445	32	312	765
17	403	221	35	371	598
18	454	323	36	337	706
19	235*	610	37	264	513
20	309	652	38	139	221
21	227	346	39	283	289
22	312	507	40	431	235
23	164	516	43	43*	624
24	326	1264	44	417	627
25	173	289	45	45	451

Front Mean 257
S.D. 145

Back Mean 474
S.D. 225

* tab failure; all others failed at metal-silicon interface.

3.62 Results of High Temperature Stress Test

A group of thirty cells was subjected to 150°C temperature for 1,008 hours. Most of these cells showed severe degradation of electrical characteristics, as shown in Table 8, and also exhibited visible lifting of the metal contacts.

Five of the cells (numbers 143, 144, 157, 170, 183) showed very little change in electrical properties, and four of these five also appeared perfect to visual inspection, while the fifth showed a small amount of contact lifting.

Tab pull strengths, shown in Table 9, averaged 124 grams, with many showing near zero strength. For the five cells listed above as showing little change in electrical properties, tab pull strengths averaged 90 grams, essentially the same as for the group as a whole. In all cases the failures occurred at the Si - Ni interface with no evidence of silicon damage.

It is possible that the performance observed at 150°C is not a fundamental property of the nickel - silicon bond,

Table 8

Electrical Characteristics of 150°C Test Cells

Cell	V_{oc}(mV)	I_{sc}(mA)	P_m(mW)	R_s(ohm)	R_{sh}(ohms)
113	543(534)	138(79)	51.5(16.0)	.482(4.14)	5263(4831)
130	580(570)	135(140)	54.0(40.0)	.330(1.64)	1587(1121)
135	586(563)	133(71)	55.5(14.0)	.312(4.33)	3508(1935)
136	575(582)	133(139)	53.0(47.0)	.328(1.18)	1447(1451)
137	565(*)	128(*)	52.5(*)	.230(*)	1664(*)
138	581(578)	136(143)	56.0(38.0)	.275(1.91)	1295(1067)
139	578(570)	131(51)	51.0(**)	.288(**)	1812(1715)
140	578(576)	136(131)	53.5(35.0)	.524(2.52)	529(500)
142	563(585)	128(130)	55.5(43.0)	.214(1.27)	1270(1451)
143	544(541)	130(137)	52.0(53.0)	.272(.329)	833(699)
144	565(574)	127(135)	52.0(52.0)	.343(.640)	971(990)
146	570(565)	136(77)	54.0(14.0)	.196(4.69)	862(1015)
147	562(515)	136(91)	51.5(17.5)	.326(3.33)	926(947)
152	583(565)	133(132)	56.0(33.5)	.270(2.29)	794(645)
153	565(543)	135(38)	50.0(**)	.489(**)	1992(1618)
155	568(557)	132(138)	54.0(43.0)	.264(1.31)	15873(15384)
156	560(572)	111(131)	44.5(42.0)	.443(1.29)	667(595)
157	550(548)	123(126)	49.5(49.5)	.293(.347)	2463(2194)
159	575(576)	137(131)	55.0(37.0)	.309(2.12)	1337(962)
161	579(543)	136(60)	56.0(**)	.285(5.59)	870(923)
162	563(567)	133(134)	55.5(37.0)	.261(2.91)	1610(1041)
163	565(556)	131(86)	53.0(18.0)	.304(4.21)	3937(3584)
168	576(566)	129(131)	52.0(45.0)	.234(.694)	575(826)
170	570(574)	134(143)	54.5(55.5)	.300(.487)	1534(1481)
172	587(576)	128(104)	54.5(27.0)	.246(3.12)	1015(943)
175	575(570)	126(132)	50.5(44.0)	.201(.963)	1026(794)
177	580(578)	124(75)	51.0(14.0)	.236(4.93)	578(571)
183	570(571)	135(142)	54.5(55.0)	.297(.467)	1163(719)
185	584(583)	124(123)	54.0(33.0)	.199(2.70)	719(641)
189	585(581)	124(74)	54.0(14.0)	.259(5.39)	826(704)
Mean	570.8 (564.8)	130.7 (111.2)	53.0 (35.3)	.300 (2.40)	1965 (1771)
S.D.	11.6 (16.6)	5.8 (32.4)	2.5 (14.1)	.084 (1.67)	2834 (2778)

Data before and (after) 1,008 hours at 150°C.

* cell broken in handling; ** too poor to measure.

Table 9

$150^{o}C$ Stress Tab Pull Strengths

	Pull Strength (g)			Pull Strength (g)	
Cell	Tab #1	Tab #2	Cell	Tab #1	Tab #2
113	193	391	155	198	145
130	0	*	156	116	*
135	57	71	157	0	335
136	0	*	159	60	*
137	0	*	161	85	96
138	23	*	162	11	113
139	57	*	163	198	*
140	0	0	168	204	*
142	0	*	170	139	136
143	0	57	172	369	*
144	147	*	175	278	193
146	145	145	177	119	*
147	411	255	183	0	0
152	113	357	185	57	*
153	170	*	189	0	*

Mean 124   S.D. 119

* bus peeled with first tab

All failures occurred at metal-silicon interface.

but rather that it is a result of contamination of the silicon surface from some process step preceding the nickel plating. Any masking technique, for example, can introduce contamination on the silicon surface which may be very difficult to remove, because cleaning techniques designed to guarantee removal of such contamination are likely to attack the chemically similar masking material as well.

3.63 Results of Thermal Shock Stress Test

A group of twenty-nine cells was subjected to 25 cycles of the thermal shock test; electrical characteristics of these cells are shown in Table 10, and results of tab pull tests are shown in Table 11.

It can be seen from the few cases in which contacts appeared to be intact that the electrical properties changed very little, even though the tab pull tests showed clearly that these contacts had, in fact, been weakened considerably. This observation suggests that the tab pull test is a more sensitive indicator of metallization integrity than are the electrical measurements.

One major point to note is the evidence of silicon damage in most of these cells, unlike the total absence of such

Table 10

Electrical Characteristics of Thermal Shock Test Cells

Cell	V_{oc}(mV)	I_{sc}(mA)	P_m(mW)	R_s(ohm)	R_{sh}(ohms)
191	559(565)	122(131)	50.0(41.0)	.304(1.839)	1427(1385)
192	558(*)	123(*)	49.0(*)	.339(*)	1042(*)
193	555(*)	124(*)	48.0(*)	.396(*)	855(*)
194	566(*)	127(*)	52.0(*)	.334(*)	704(*)
195	574(577)	129(131)	50.0(34.0)	.313(2.360)	521(452)
196	580(582)	126(133)	52.0(54.0)	.288(.336)	442(263)
197	548(553)	119(125)	46.5(46.0)	.339(.581)	137(123)
198	530(*)	120(*)	44.5(*)	.516(*)	295(*)
199	565(*)	127(*)	44.5(*)	.574(*)	543(*)
202	516(*)	112(*)	39.5(*)	.518(*)	1299(*)
203	548(*)	116(*)	43.5(*)	.259(*)	49(*)
204	546(552)	122(126)	50.0(36.5)	.264(2.522)	379(347)
206	573(584)	126(132)	51.0(44.5)	.302(1.305)	254(181)
207	551(552)	121(118)	50.0(33.0)	.241(2.462)	195(185)
208	553(*)	124(*)	48.0(*)	.441(*)	806(*)
211	548(*)	123(*)	47.0(*)	.526(*)	575(*)
212	558(*)	124(*)	45.5(*)	.416(*)	220(*)
214	579(*)	130(*)	53.5(*)	.329(*)	1250(*)
219	522(*)	119(*)	45.0(*)	.405(*)	2000(*)
220	552(569)	124(131)	49.0(46.0)	.358(.802)	1190(820)
222	549(556)	117(124)	47.0(45.5)	.278(.648)	100(99)
224	528(530)	121(111)	47.0(29.0)	.287(2.337)	1389(1393)
226	542(540)	114(109)	43.0(36.0)	.241(.794)	81(84)
227	545(*)	122(*)	47.5(*)	.405(*)	232(*)
233	546(*)	121(*)	47.0(*)	.406(*)	220(*)
236	570(*)	126(*)	52.5(*)	.278(*)	362(*)
238	578(*)	134(*)	52.0(*)	.371(*)	855(*)
239	544(*)	119(*)	45.5(*)	.464(*)	266(*)
242	580(*)	135(*)	55.0(*)	.357(*)	4545(*)

* unable to measure

Data before and (after) Thermal Shock Stress.

Table 11

Thermal Shock Stress Tab Pull Strengths

Cell	Pull Strength (g) Tab #1	Pull Strength (g) Tab #2	Cell	Pull Strength (g) Tab #1	Pull Strength (g) Tab #2
191	28	---*	211	---*	---*
192	---	---*	212	---	---*
193	---	---	214	---*	---*
194	---*	---	219	0*	85*
195	28*	---*	220	28*	99*
196	170*	0*	222	0*	---*
197	28*	0*	224	---*	57*
198	43*	---	226	0*	0*
199	---*	---*	227	---*	---*
202	---*	---	233	---	---*
203	---*	---*	236	---	---
204	0*	---*	238	---*	227*
206	---*	28*	239	---*	---*
207	0*	---*	242	---*	---*
208	---*	---*			

--- bus lifted at tab during thermal shock cycling.

* silicon damage evident; all others failed at silicon - nickel interface.

Some degree of lifting of back solder was evident in fifteen of the cells.

damage in the cells subjected to the high temperature and bias - temperature - humidity stresses, and the fact that this silicon damage occurs during the thermal shock cycles without the application of any external mechanical stress.

Another group of cells, fabricated using a different masking technique, was also subjected to the thermal shock test, and the results were essentially identical.

In an additional experiment, buses were formed on diffused and alloyed silicon using Kapton tape as a masking material for the nickel plating. Using this technique, the masking process does not contaminate the surface of the silicon to be plated. The tape was removed prior to solder dipping. These specimens were then subjected to the thermal shock test.

Nearly all of the buses lifted during the thermal shock stress, and in every case the silicon was damaged over the entire area under the bus. Silicon damage in the regular cells was not that extensive, suggesting that the masking process does contribute some degree of contamination to the silicon surface.

3.64 Results of Thermal Cycle Stress Test

A group of thirty cells was subjected to a thermal cycle stress alternating between -65°C and +150°C in air for 100 cycles. In every case the bus peeled 100% or nearly 100%. In some cases the contact failure was evident early in the test.

No electrical measurements or tab peel tests could be conducted on these cells after the stress test.

In general the metal separation occurred at the Si - Ni interface, with evidence of some separation at the nickel - solder interface in eight cells, and some silicon damage, ranging from a single small pit to about 70% of the bus area, was apparent in twenty-one of the cells.

3.65 Results of Control Cells

A group of 100 cells was stored in nitrogen at room temperature for about ten weeks as a control group. Electrical data from these cells are shown in Table 12.

Tab pull strengths of these cells averaged 177 grams. Of the 200 tabs, 7 failed at the tab - solder joint, 32

Table 12

Electrical Characteristics of Control Cells

Cell	V_{oc}(mV)	I_{sc}(mA)	P_m(mW)	R_s(ohm)	R_{sh}(ohms)
50	591(586)	129(135)	52.5(54.5)	.306(.297)	78(78)
51	576(568)	133(137)	56.0(55.5)	.216(.294)	323(300)
53	563(558)	129(132)	40.0(40.0)	.100(.059)	9(9)
54	573(564)	132(135)	52.5(52.0)	.327(.351)	870(408)
55	550(538)	126(127)	50.0(49.0)	.261(.233)	100(95)
56	581([illegible]70)	135(130)	54.5(54.5)	.377(.261)	746(680)
57	579([illegible]9)	138(141)	55.0(56.5)	.464(.288)	654(617)
58	555(542)	130(127)	39.0(33.5)	.211(.487)	17(16)
59	590(580)	137(136)	57.5(56.5)	.361(.312)	2336(1828)
60	546(536)	131(135)	52.0(52.0)	.308(.274)	294(234)
61	576(565)	128(130)	54.0(53.0)	.235(.253)	478(420)
62	581(571)	133(134)	55.0(55.0)	.265(.265)	166(160)
63	563(550)	133(137)	48.0(48.0)	.297(.392)	45(43)
64	585(573)	134(138)	52.5(54.0)	.424(.332)	6993(1592)
65	572(563)	134(135)	53.5(53.0)	.315(.344)	806(538)
66	589(580)	127(128)	53.5(52.0)	.239(.316)	7874(8197)
67	550(539)	122(124)	50.5(50.0)	.248(.205)	585(546)
68	565(553)	133(136)	52.5(52.0)	.321(.317)	1709(1294)
69	573(570)	129(138)	52.0(54.0)	.241(.300)	588(442)
70	578(570)	137(140)	56.5(57.0)	.312(.314)	184(172)
71	548(538)	132(134)	53.0(53.0)	.261(.284)	472(410)
72	595(584)	125(128)	54.0(54.0)	.288(.265)	472(448)
73	571(565)	127(132)	55.0(56.0)	.213(.233)	2732(2525)
74	581(575)	122(131)	50.0(52.0)	.238(.262)	56(53)
75	577(573)	128(137)	53.0(56.0)	.261(.266)	234(227)
76	573(569)	119(127)	50.0(53.0)	.287(.262)	2618(2053)
77	586(585)	123(130)	52.0(54.0)	.259(.286)	787(714)
78	568(566)	125(131)	47.5(47.0)	.213(.379)	45(43)
79	551(548)	131(139)	46.5(49.5)	.299(.296)	30(29)
80	545(536)	120(127)	47.0(49.0)	.351(.316)	244(230)
81	543(536)	127([illegible]5)	50.5(51.5)	.268(.264)	694(595)
83	577(571)	121(132)	51.0(55.0)	.229(.269)	862(725)
84	573(565)	119(126)	50.5(52.0)	.257(.267)	303(291)
85	534(527)	133(141)	44.5(46.0)	.701(.709)	146(142)
86	572(567)	131(139)	52.5(54.5)	.285(.334)	820(662)
87	579(575)	124(132)	52.0(52.0)	.247(.474)	171(163)
88	585(580)	122(127)	49.5(51.5)	.291(.280)	86(83)
90	570(562)	117(126)	49.0(52.0)	.272(.286)	667(641)

Electrical Characteristics of Control Cells

Cell	Voc(mV)	Isc(mA)	Pm(mW)	Rs(ohm)	Rsh(ohms)
91	572(562)	125(129)	52.5(52.5)	.324(.332)	1020(980)
92	573(566)	127(127)	53.0(52.0)	.274(.276)	1232(990)
93	549(538)	124(122)	51.0(48.0)	.206(.333)	315(286)
94	579(570)	128(130)	51.5(51.0)	.312(.318)	2083(1538)
95	583(581)	129(132)	54.0(54.5)	.310(.361)	1064(1068)
96	565(556)	122(125)	48.5(48.0)	.378(.402)	800(714)
97	548(538)	126(127)	51.0(50.0)	.294(.287)	259(243)
98	573(566)	136(135)	56.0(54.0)	.274(.301)	606(532)
99	574(566)	126(127)	52.5(51.5)	.258(.280)	5525(3401)
100	579(572)	140(143)	56.0(56.0)	.302(.317)	662(613)
115	585(576)	135(141)	57.0(57.0)	.341(.323)	314(298)
116	575(569)	136(141)	55.0(55.5)	.300(.340)	1730(1285)
117	582(572)	128(132)	52.5(52.0)	.252(.248)	158(149)
118	580(574)	125(130)	52.5(53.5)	.277(252)	1043(877)
119	582(577)	130(135)	54.5(55.0)	.207(.237)	556(400)
120	578(568)	135(141)	52.0(53.0)	.424(.485)	690(581)
121	565(557)	129(131)	40.5(40.0)	.391(.411)	34(33)
122	579(576)	131(140)	51.0(54.0)	.329(.337)	108(99)
123	595(589)	132(138)	57.5(58.5)	.298(.290)	1247(1034)
124	581(575)	128(131)	53.0(52.0)	.272(.310)	314(299)
126	540(538)	135(141)	48.0(49.0)	.522(.545)	60(58)
128	579(577)	126(134)	54.0(56.5)	.246(.256)	441(490)
129	576(573)	126(129)	50.0(50.0)	.339(.305)	125(121)
131	577(570)	128(131)	53.0(53.0)	.240(.282)	250(234)
133	586(576)	126(129)	51.5(51.5)	.253(.250)	212(195)
145	588(582)	127(130)	52.0(52.0)	.251(.267)	75(70)
148	570(563)	132(136)	52.0(54.0)	.412(.353)	3257(2841)
149	565(558)	135(139)	53.0(53.0)	.239(.275)	680(599)
150	578(568)	126(132)	54.0(54.0)	.245(.201)	232(221)
151	566(560)	133(135)	52.0(51.0)	.281(.262)	197(181)
154	580(576)	132(137)	55.0(54.5)	.257(.269)	170(166)
158	570(569)	133(138)	52.0(54.0)	.401(.290)	334(316)
160	567(567)	131(134)	51.0(51.0)	.307(.311)	306(267)
164	580(573)	130(133)	54.5(54.0)	.243(.240)	3322(1795)
165	590(583)	137(141)	57.0(58.0)	.332(.336)	3759(2941)
166	546(542)	122(122)	50.5(49.5)	.225(.237)	439(385)
167	592(581)	128(134)	57.0(57.0)	.172(.188)	4237(2551)
169	595(586)	129(134)	56.5(56.0)	.282(.278)	1949(1276)

Electrical Characteristics of Control Cells

Cell	V_{OC}(mV)	I_{SC}(mA)	P_m(mW)	R_s(ohm)	R_{sh}(ohms)
171	564(555)	133(135)	51.0(49.0)	.327(.299)	60(55)
173	574(573)	136(142)	55.5(56.0)	.326(.307)	503(364)
174	587(575)	130(129)	56.0(54.0)	.222(.226)	377(364)
176	579(569)	133(135)	53.0(51.0)	.289(.347)	413(345)
178	568(561)	126(123)	42.0(39.5)	1.006(1.023)	51(53)
179	569(565)	125(128)	50.5(50.0)	.266(.340)	397(327)
181	563(558)	135(138)	52.0(52.5)	.307(.287)	322(302)
182	579(577)	134(137)	54.5(54.0)	.373(.312)	307(266)
184	559(550)	138(143)	55.0(55.0)	.342(.371)	532(500)
188	560(557)	130(134)	45.0(43.5)	.346(.315)	286(278)
190	568(563)	121(124)	50.5(50.0)	.253(.269)	200(184)
1101	572(560)	132(134)	56.0(55.0)	.258(.277)	6369(4425)
1102	564(551)	138(139)	51.0(50.0)	.458(.444)	1502(1290)
1103	568(558)	132(137)	52.5(53.5)	.358(.306)	1553(1466)
1104	581(573)	125(126)	49.0(48.5)	.364(.298)	109(104)
1105	537(577)	136(137)	57.0(56.0)	.280(.301)	909(709)
1106	582(571)	133(138)	54.0(54.0)	.310(.321)	505(459)
1107	557(548)	139(142)	54.5(54.0)	.366(.378)	1116(1024)
1108	560(549)	135(138)	42.0(42.0)	.279(.120)	15(14)
1109	588(576)	130(130)	55.0(53.0)	.249(.290)	2933(2000)
1110	572(564)	126(129)	51.0(52.0)	.334(.292)	571(490)
1111	590(575)	143(136)	60.5(56.5)	.364(.385)	1244(1157)
1112	588(577)	129(133)	53.0(54.0)	.355(.280)	4808(2558)
1135	557(546)	139(142)	52.0(51.5)	.356(.353)	3509(3257)
Mean	572.4 (564.9)	129.8 (133.4)	52.0 (52.1)	.307 (.314)	1047 (798)
S.D.	13.4 (13.7)	5.3 (5.3)	3.8 (4.1)	.104 (.106)	1530 (1134)

Data before and (after) approximately ten weeks storage at room temperature in a nitrogen atmosphere.

failed at the nickel-solder interface, and the remainder failed at the silicon-nickel interface. There was no apparent silicon damage in any case.

3.7 Additional Thermal Stress Tests

The specified thermal stress tests show that the nickel/solder metallization on silicon does not survive the temperature extremes of -65°C and +150°C, but they give no indication of what temperature range might be tolerable. As a consequence, additional experiments were conducted to determine approximately what temperature limits might be acceptable for this kind of metallization.

3.71 Thermal Shock Tests

A number of exploratory thermal shock experiments were conducted over several different temperature ranges using tab pull strength measurements to assess the quality of the metallization. As usual there was variation in the results, but it appeared that a temperature range of -40 to +100°C was quite tolerable, and a carefully controlled thermal shock experiment was conducted using this range.

Single crystal silicon wafers (1-0-0, p-type, 0.2-5.0 ohm-cm) were etched in 25% NaOH at 97°C for seven minutes,

rinsed in HCl for five minutes, treated with 20:1 aqueous HF, rinsed in de-ionized water and dried. The wafer surfaces were converted to n-type by phosphorus diffusion, and the wafers were once again treated with 20:1 aqueous HF until hydrophobic, then rinsed with de-ionized water and dried. Sheet resistances averaged about 34 ohms/square.

A pattern of buses, each bus about 2 mm wide, was formed on the wafers with Kapton tape, and nickel was plated at 85°C for five minutes from the electroless nickel plating solution described in Appendix B. The Kapton tape was removed and the wafers were dipped in molten solder. The wafers were cut into smaller pieces and tinned copper tabs, 1.75 mm wide, were soldered to the buses. Pull strengths were measured on several of the tabs (control group) and several more were subjected to a 25 cycle thermal shock regimen as described in Section 3.53, but using -40°C and +100°C as the low and high temperatures.

The control group (34 tabs) showed a mean tab pull strength of 431 g (standard deviation 248 g) while the thermal shock group (43 tabs) had a mean strength of 384 g (standard deviation 165 g). The difference of 11% is small, much less than a single standard deviation.

3.72 High Temperature Test

Another group of wafers with tabs, prepared in the same way and at the same time as those described in the preceding section, were kept in an oven at 100°C for 763 hours, and the tabs were then pulled as before. This group (48 tabs) showed a mean tab pull strength of 453 g (standard deviation 282 g), a result almost identical to that of the control group.

3.8 Summary of Environmental Stress Tests

The cells survived the bias - temperature - humidity test perfectly.

The temperature extremes of -65°C and +150°C are too severe for these cells, but metallization survives well at -40°C and +100°C.

In several cases, where tab pull strengths showed that adhesion had degraded substantially, electrical measurements showed no change.

Different modes of failure were observed with different kinds of stress. In cells from the bias - temperature - humidity and high temperature test, as well as in the control group, failure was almost exclusively at the Si - Ni

interface with no evidence of silicon damage. Cells from the thermal cycle test failed predominantly at the Si - Ni interface, with some showing evidence of silicon damage, while failures in the thermal shock group occurred predominantly in the silicon.

4. NICKEL PENETRATION OF SILICON

In this task electron microprobe analysis is used in an effort to detect any diffusion of nickel into silicon as a result of sintering.

4.1 Silicon Preparation and Plating

Silicon wafers with phosphorus front diffusion were plated with nickel using the Solarex electroless nickel plating process (but with no pattern on the front surface).

4.2 Sintering

Several 1 cm squares were cut from the processed wafers and were sintered in an inert atmosphere (He or N_2) for varying times at temperatures from 200°C to 450°C.

Specimens sintered at 350°C and higher, cooled in the inert atmosphere, then exposed to air, peel when exposed to air. Nickel is adhering tightly when first exposed to air, and then peels gradually with time, beginning at the edges. Measurements of the surface resistivity of the silicon after peeling show very low values of resistivity, indicating that the remaining surface contains some nickel.

A phase change is reported to occur at 325°C in plated nickel films containing phosphorus. (4,5) The initial state

is reported to be a highly disordered solid solution of phosphorus in nickel, while heat treatment above 325°C produces two crystalline components, tetragonal Ni_3P and fcc Ni.

4.3 Specimen Preparation for Microprobe Analysis

A procedure was developed for mounting and angle lapping specimens for microprobe analysis. Specimens were mounted in Buehler Castolite (a polyester) and were lapped at an angle of 3.5° using successively finer grits down to 0.05 micron alumina for the final polishing.

4.4 Electron Microprobe Analysis

Several selected specimens were delivered to Tousimis Research Laboratory for electron microprobe analysis. Specimens selected had been sintered at the following temperatures and times:

200°C, 1 min (2 specimens)

300°C, 15 sec, 1 min, 2 min (2 specimens)

425°C, 12 min

450°C, 1 min, 2 min, 20 min, 30 min, 40 min.

Figure 3 shows a microprobe scan as well as a schematic diagram of the scan. It can be seen that the probe detects silicon through the nickel (the silicon trace does not go to

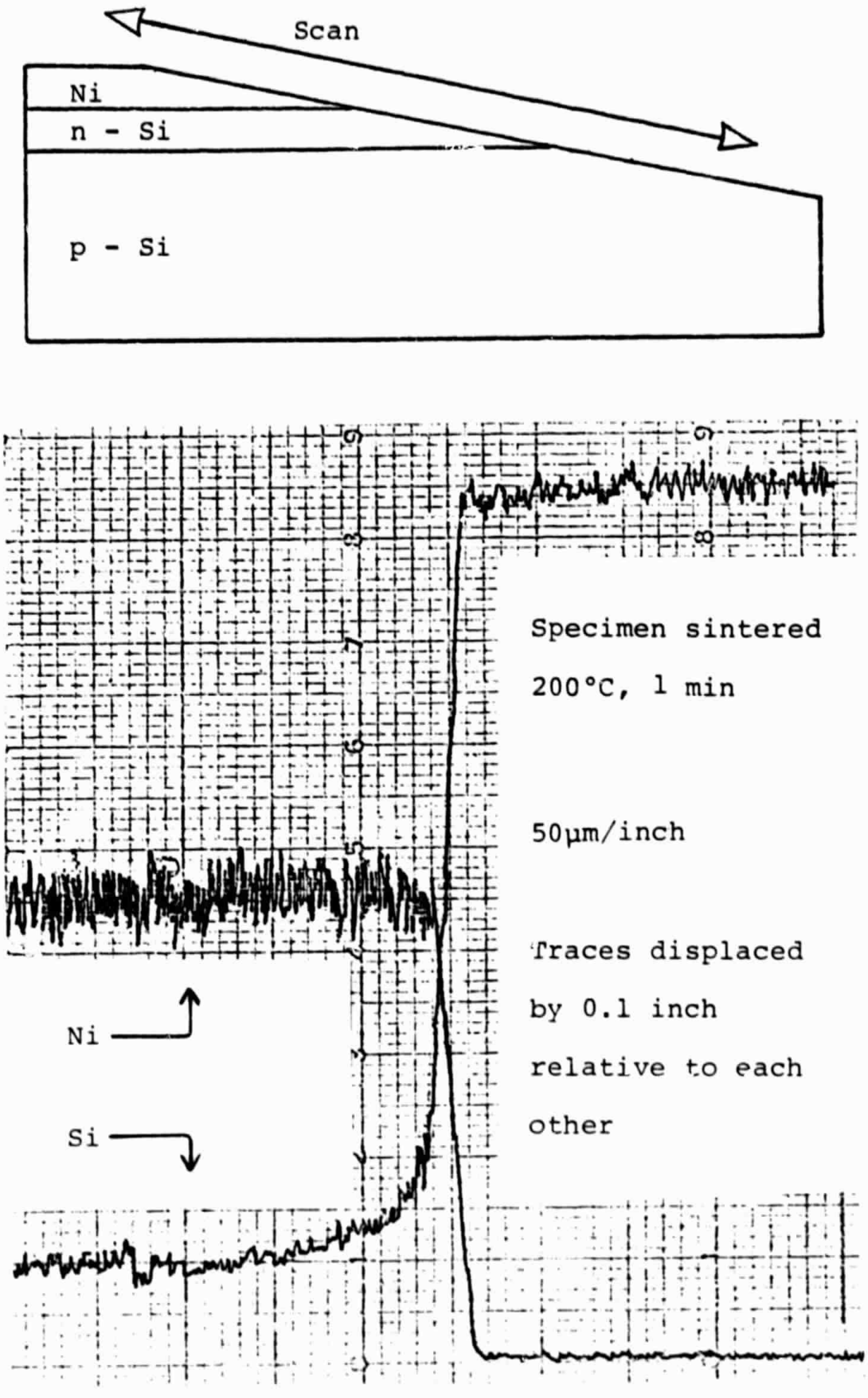


Figure 3. Electron Microprobe Analysis: Schematic of scan (above); data from a typical scan (below).

zero) and that the transition from silicon to nickel occurs over 10-15 microns of scan length (1 micron of depth is equivalent to 16.38 microns of scan length). This transition region is the region where nickel thickness is varying and the probe is detecting more silicon through the thinner nickel. Electron beam diameter was 1 micron.

The scan shows no evidence of nickel penetration of silicon, and it is typical of all of our scans until we reach the lengthier sintering times (20, 30, 40 min) at 450°C. In these latter scans we see the transition region expanding into the 100-200 micron range, indicating nickel penetration depths up to about 12 microns. Figure 4 presents an example of a microprobe scan of one of these specimens sintered for a long time at high temperature.

These observations are consistent with reverse bias dark leakage currents previously reported and outlined here in Figure 5, which showed little increase in leakage current after sintering for as long as 30 min at 350°C or 2 min at 450°C, but a very substantial increase after 3 min at 450°C.

It is also evident from the nature of the microprobe data that any penetration of the p-n junction by nickel will be detected earlier by electrical current leakage measurements than by electron microprobe scans.

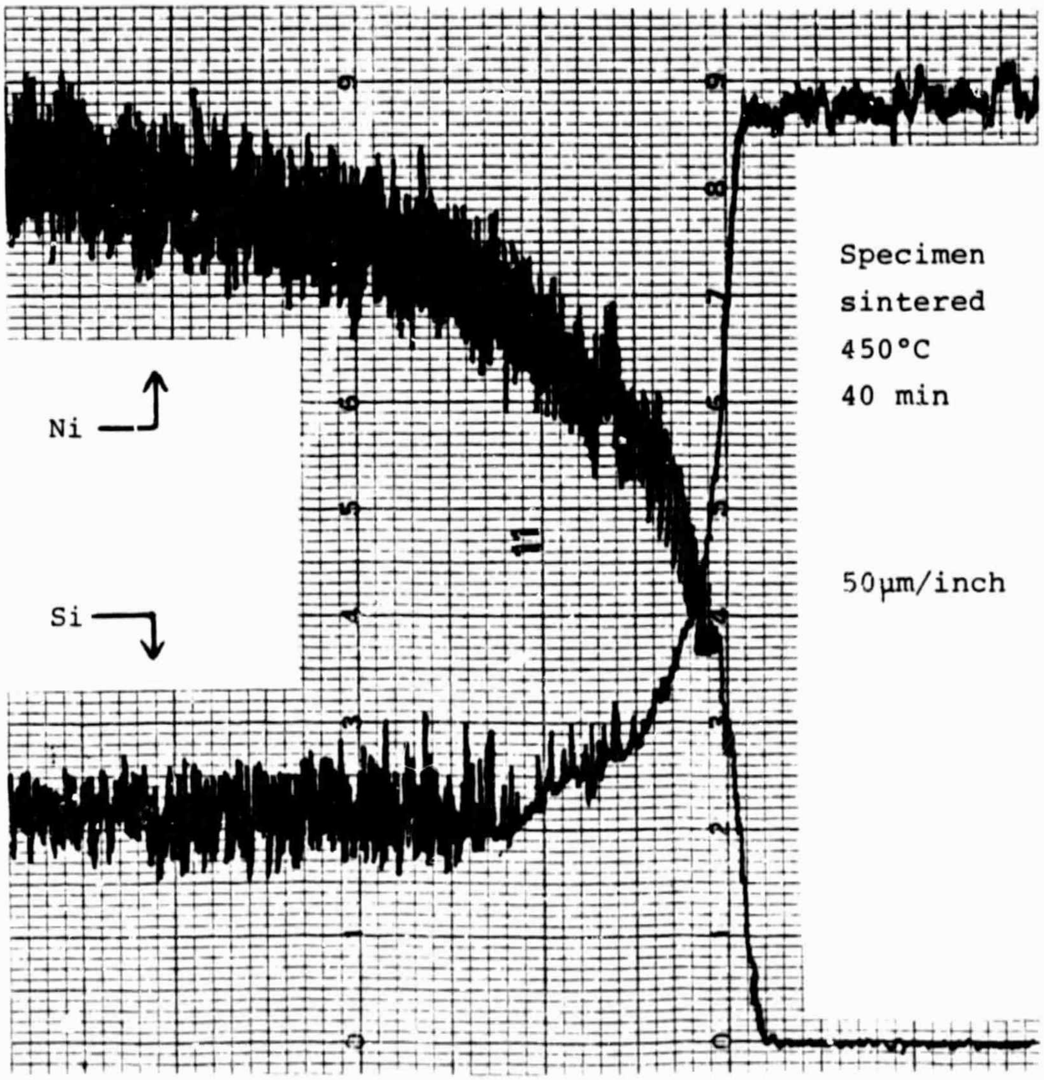
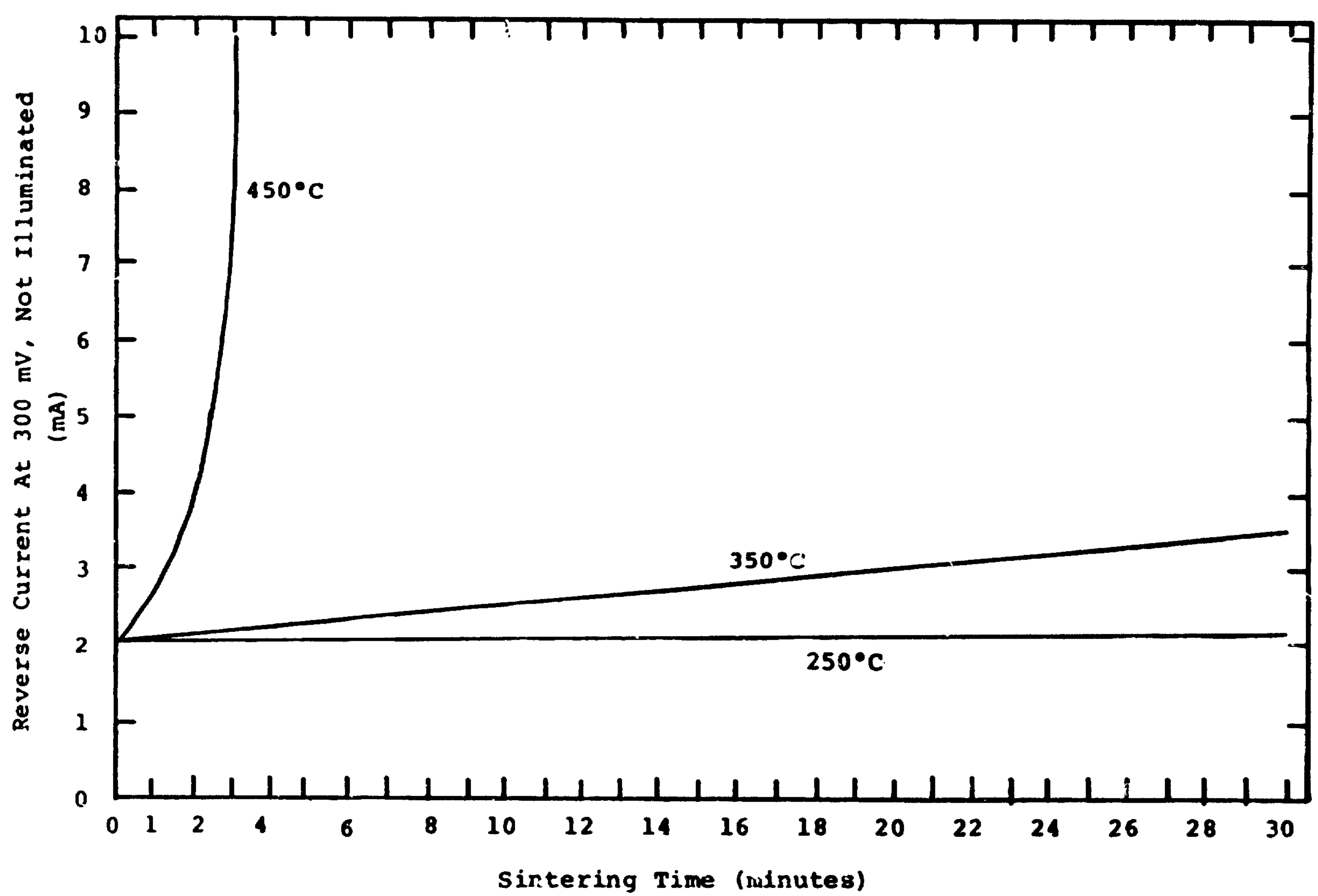


Figure 4. Electron microprobe scan of specimen sintered for 40 min at 450°C.

Figure 5. Nickel Sintering and Leakage Current



5. EFFECT OF NICKEL PLATING SOLUTION ON SOLAR CELLS

A number of solar cells were fabricated in which nickel plating time was varied from four to fourteen minutes. Our standard electroless nickel plating solution was used at a temperature of 90°C. The cells are 2 cm squares cut from larger wafers and have a bus, about 1 mm wide, parallel to and close to one edge with six narrower conducting fingers perpendicular to the bus. These cells are essentially the same as the ones pictured and described earlier.

5.1 Light I-V Characteristics

Measurements of light I-V characteristics have been made at AMO, and the data are shown in Table 13. Cells within each group were plated in three separate batches (e.g. the group of 11 cells with a 10 minute plating time comprises cells plated in three separate batches on three different occasions).

Little variation is seen in open circuit voltages, but the short circuit current and maximum power data show distinctly better cell quality resulting from the intermediate plating times (6-10 min), and this trend is especially obvious in series resistances.

Table 13

Influence of Nickel Plating Time on Electrical Characteristics of Cells

	Plating Time (Min)					
	4	6	8	10	12	14
V_{oc} white mV	559 (8)	561 (12)	566 (13)	569 (17)	565 (14)	574 (10)
V_{oc} red mV	542 (9)	545 (12)	550 (13)	552 (15)	548 (14)	557 (10)
V_{oc} blue mV	508 (11)	507 (16)	520 (13)	518 (20)	512 (22)	515 (20)
P_m white mW	45.6 (3.1)	49.8 (3.0)	51.7 (2.7)	51.5 (3.0)	45.1 (6.6)	46.3 (3.3)
P_m red mW	25.4 (1.9)	27.7 (1.1)	28.7 (2.4)	27.9 (1.7)	24.7 (5.1)	26.0 (2.8)
I_{sc} white mA	114.7 (8.7)	121.6 (4.6)	121.9 (3.5)	121.8 (3.3)	110.1 (13.5)	113.7 (2.7)
I_{sc} red mA	65.4 (3.1)	70.4 (3.3)	69.4 (3.4)	68.9 (1.7)	62.5 (8.9)	66.4 (1.7)
I_{sc} blue mA	26.7 (2.7)	25.4 (2.3)	28.1 (1.7)	26.6 (3.2)	24.9 (2.4)	24.0 (0.8)
R_{series} ohm	.279 (.145)	.209 (.077)	.179 (.047)	.168 (.053)	.249 (.137)	.266 (.084)
No. of Cells	8	9	13	11	18	11

Mean values and (standard deviations)

AMO 2 cm square cells

Cells plated for less than four minutes could not be solder coated successfully, and cells plated for 12 min or 14 min had obviously poorer contact adhesion than those plated for shorter times. In fact, front metallization lifted spontaneously from three cells plated for 14 min (electrical measurements were not made on these three cells).

These light I-V data do not suggest any cell deterioration resulting from exposure to the plating solution. The observations are best explained in terms of contact quality, with intermediate nickel thicknesses being obviously most desirable.

5.2 Dark I-V Characteristics

Measurements have also been made of forward and reverse dark I-V characteristics. Diode n-factors obtained from these data are shown in Table 14. This is an effective n-factor defined by the instantaneous slope at the maximum power point of a plot of log I (dark) versus V.

Table 14

Diode n-Factors

	Plating Time (Min)					
	4	6	8	10	12	14
n-Factor	1.86	1.93	1.75	1.83	1.80	1.98
(Std Dev)	(0.08)	(0.21)	(0.28)	(0.25)	(0.24)	(0.31)

Some variation is obvious in the data of Table 14, but there is clearly no trend with plating time. The n-factors have also been calculated from measurements of static V_{oc} and I_{sc} made at varying light levels, and, while the values are slightly different than those shown in the table, there is still no evidence of a trend with plating time.

Thus we conclude that the cell properties are not affected by exposure to the plating solution in a time range from 4 to 14 minutes, except for the effect of nickel thickness on contact quality.

This kind of experiment cannot, of course, tell anything about interactions which may occur between the cell and the solution before nickel deposition has begun.

5.3 Etching of Silicon by Plating Solution

Some of our observations from experiments comparing the Motorola process with single step electroless nickel plating caused us to suspect that the plating solution was etching silicon before depositing any nickel. We confirmed this suspicion by measuring changes in sheet resistivities and open circuit voltages caused by the plating process. Results of these experiments are reported in Section 6.3.

We have also performed gravimetric experiments to make a more direct determination of the quantity of silicon removed during the plating process (and, incidentally, of the quantity of nickel plated).

Eight polished wafers, 2 1/4" diameter, Cz, p type, 1-0-0, 0.2 - 5.0 ohm-cm, were diffused (phosphine) to a sheet resistivity of about 50 ohms/square (both sides). The wafers were then treated with piranha etch (2 parts conc H_2SO_4, 1 part 30% H_2O_2), rinsed in distilled water, dried, and weighed to the nearest 0.1 mg. The wafers were next plated in the electroless nickel plating solution at 90°C, four of them for 6 min, and four of them for 12 min, after which they were rinsed again in distilled water, dried and weighed again. The nickel was then removed by piranha etch and once again the wafers were rinsed in distilled water, dried and weighed.

The difference between the second and third weighings is assumed to be the weight of plated nickel, while the difference between the first and third weighings is assumed to be the weight of silicon etched away by the plating solution. This silicon weight loss includes any oxide which may have been present, while the nickel weight includes some phosphorus which is contained in the nickel. We have also determined that piranha treatment of the bare diffused wafer causes no weight change.

Data from the eight wafers are shown in Table 15. Thickness calculations were made using 51.9 cm^2 as the wafer area (two sides plus the edge), 2.33 g/cu cm as the density of silicon and 8.90 g/cu cm as the density of nickel. Variations in the weight of silicon lost are relatively large, because we are operating at the limit of the balance's capability.

Table 15

Effect of Electroless Ni Plating at 90°C

Plating Time (min)	Wafer No.	Wt. of Si Lost (g)	Thickness of Si Lost (micron)	Wt. of Ni Plated (g)	Thickness of Ni (micron)
6	1	0.0014	0.12	0.0214	0.463
6	2	.0014	.12	.0211	.457
6	3	.0011	.09	.0207	.448
6	4	.0024	.20	.0208	.450
6	AVG		0.13		0.454
6	S.D.		0.05		0.007
12	5	0.0012	0.10	0.0409	0.886
12	6	.0008	.07	.0417	.903
12	7	.0019	.16	.0418	.905
12	8	.0014	.12	.0416	.900
12	AVG		0.11		0.899
12	S.D.		0.04		.009

While our deviations are relatively large in amounts of silicon lost, the length of plating obviously has no effect. This is consistent with a mechanism in which silicon etching occurs rapidly before nickel plating begins and ceases once the nickel has begun to deposit.

The nickel data are very consistent, showing very small deviations, and with the 12 minute plate producing almost exactly double the thickness of the 6 minute plate.

We next performed a similar experiment in which portions of the wafers were masked with Kapton tape during the plating process, expecting to produce a step on the surface of the wafer which could be measured by profilometry, but we were unable to detect any step.

Scanning electron micrographs were obtained on some of these specimens, and these showed a clear difference, with an apparent step, between the masked and plated areas. One of these micrographs is shown in Figure 6. The Kapton tape mask and residual adhesive were removed prior to stripping the nickel.

5.4 Staining of Silicon

In Section 2.1 we reported the appearance of stains on silicon after dissolution of the silicon dioxide. Similar stains have frequently been reported to have occurred as a result of etching silicon or removing oxide under a variety of conditions. We also sometimes observe such stains on silicon after chemically removing electroless nickel metallization and also after peeling nickel-solder metallization from silicon.

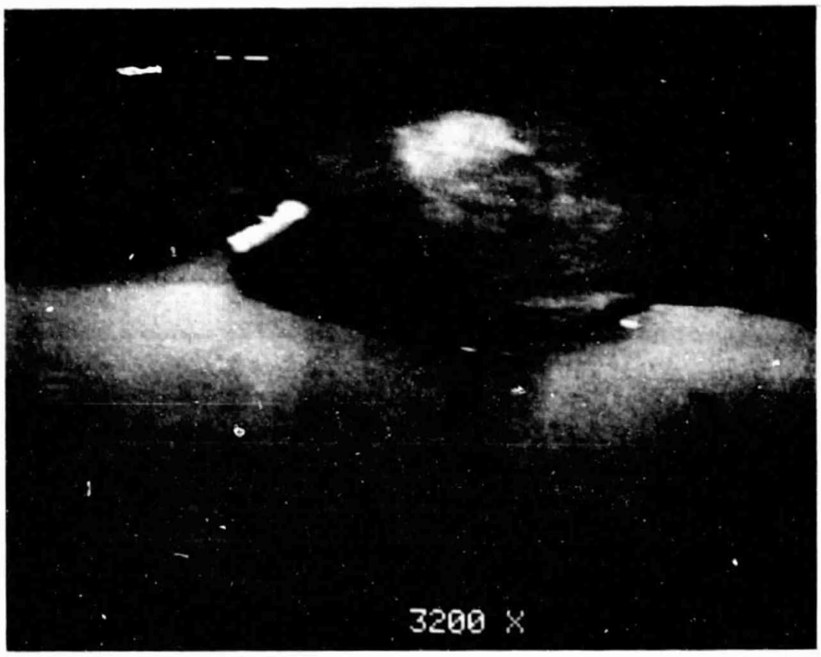
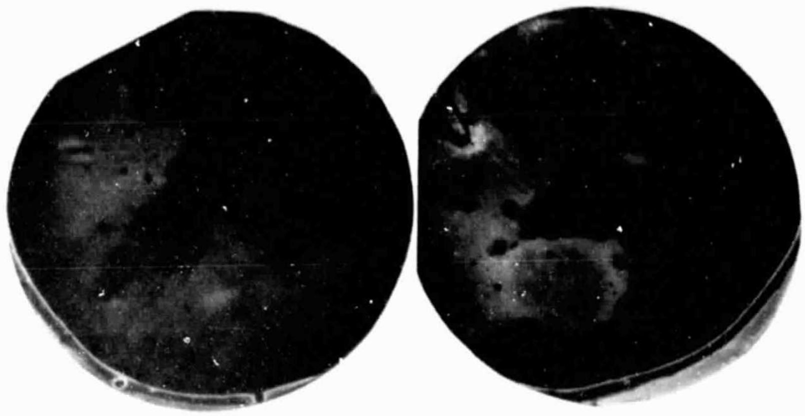
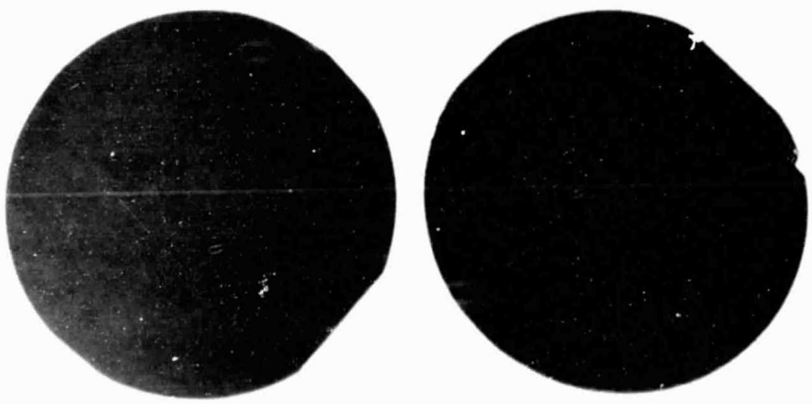


Figure 6. Scanning electron micrograph of silicon after plating and stripping nickel. Upper (dark) area was masked during plating; lower (light) area had nickel plate.

It occurred to us that the staining might vary with the surface conductance of the silicon, and we consequently diffused (phosphine) a number of polished silicon p-type wafers to different levels of sheet resistivity, plated them and removed the nickel with piranha etch. There was a very clear dependence of staining on sheet resistivity, and examples are shown in Figure 7. The stains appear lighter than the silicon, and it can be seen that wafers with a sheet resistivity of 22 ohms/square show no staining, while wafers having a sheet resistivity of 120 ohms/square show extensive staining.



Sheet resistivity 120 ohms/square



Sheet resistivity 22 ohms/square

Figure 7. Silicon staining caused by electroless nickel plating.

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6. MOTOROLA PROCESS

The Motorola process is a complex one; it utilizes the standard electroless nickel plating solution of Brenner and Riddell (3,4), but it precedes the electroless nickel plating step with three steps of immersion palladium plating, one step of electroless palladium plating, two heat treatment steps and several cleaning and rinsing steps.

The Motorola process specification, as supplied by Motorola to JPL, is included herein as Appendix B.

The specification defines twenty-eight steps, exclusive of the solder dipping operation, and requires one hour and forty-nine minutes, not including any time for transfer, inspection, cooling and drying operations. This is an extremely lengthy process relative to a single step nickel plating process, and we have been most forcibly impressed by the cumbersome, time consuming nature of the process.

6.1 Reliability and Reproducibility

The major purpose of the complex processing prior to the nickel plating step is to assure repeatable and reliable metallization of the solar cells, by eliminating or minimizing any effects of prior processing of the silicon.

We have run the Motorola process many times with variable results. Metallization sometimes lifts spontaneously from the silicon before the process has been completed, frequently during the electroless palladium plating step, and it sometimes works very well, giving an adherent, good looking plate. Thus, it appears to us that success of the Motorola process is at least as dependent upon prior history of the specimen as is the simple electroless nickel plating process.

In an effort to improve repeatability of the process, we have tested several preliminary specimen treatments, and have chosen to use a piranha etch (1 min in a mixture of 2 parts conc H_2SO_4 and 1 part 30% H_2O_2) followed by a deionized water rinse and spin drying, because it appears to aid in achieving reasonably reproducible results.

Our second general observation, then, is that the Motorola process is not the highly reproducible and reliable process it was intended to be, and this fact is recognized by Motorola in the caveat, quoted previously, that the "process .... may require minor modifications to account for different types of solar cell substrates and .... the previous processing history of substrates...."

6.2 ETCHING OF SILICON BY PLATING SOLUTIONS

We reported previously (6) that the electroless nickel plating solution can dissolve silicon dioxide. We are also aware that the electroless nickel and palladium plating solutions can etch silicon if they are not plating metal, and that the immersion palladium plating solution also removes some silicon.

To detect any possible effects of etching, we measured sheet resistances and illuminated open circuit voltages of several cells prior to metallization, then plated them, removed the metallization, and measured these parameters again. Piranha etch removed all of the nickel and most of the palladium, but traces of palladium appeared to remain; treatment with aqua regia for 2 minutes removed all of the metal. Results of this experiment are shown in Table 16.

Table 16

Electrical Parameters Before Plating and After Stripping of Metallization

	Illuminated V_{OC} (mV)		Sheet Resistance (ohms/□)	
	Before	After	Before	After
Motorola				
Range	543-583	298-468	54-55	310-360
Mean	567	373	55	335
Ni Only				
Range	536-591	467-547	54-55	57-67
Mean	555	509	55	61

Sheet resistances, originally 54-55 ohms per square, measured 57-67 ohms per square in the group plated with nickel only, but had increased to 310-360 ohms per square in the group plated using the Motorola process.

Illuminated open circuit voltages decreased in all cases, but the change was relatively small in the cells plated with nickel only and was large in the cells plated by the Motorola process.

We concluded that some silicon was etched in these plating processes, and that the Motorola process removes more silicon than does the simple electroless nickel plating process. Thus it appears that a deeper diffusion is required for the Motorola process.

6.3 TAPE PEEL TEST

A group of 2" diameter round polished silicon wafers (Cz, p-type, 1-0-0, 0.2-5 ohm-cm) was given the piranha pre-treatment followed by phosphine diffusion, glass removal by dilute HF, aluminum back alloy, and removal of excess aluminum by cold conc HCl.

Half of the cells were plated using the Motorola process, and the other half were plated using only the electroless nickel plating step of the Motorola process. Adhesion of the metallization was tested by pressing adhesive tape to the metal and peeling it off.

The adhesion was quite good in all cases with only small amounts of metal lifting near edges or in very small isolated spots. We estimate 98-99% adherence to the specimens plated with nickel only and 99+% adherence to the specimens plated by the Motorola process.

We interpret these observations as indicating essentially identical behavior in the two groups.

6.4 TAB PULL TEST

Another group of silicon wafers was prepared as before (piranha, diffusion, alloying, cleaning) and portions of the group were plated using a) the Motorola process, b) the electroless nickel plating step of the Motorola process, and c) the electroless nickel plating solution of the J.E. Halma Company. We have used the proprietary Halma solution extensively, and, while we do not know its composition, we believe it is similar to the Brenner solution used by Motorola.

A pattern of buses, about 1 mm wide, was formed on the cells and the cells were dipped in molten solder after plating. Tinned copper tabs, 1.75 mm wide, were soldered to the buses, and 90° tab pull tests were conducted. Some of the specimens having nickel only were sintered for 1 min at 250°C prior to solder dipping. The Motorola process, of course, incorporates heat treatment steps.

Results of the tab pull tests are shown in Table 17. The adhesion is clearly poorest in the group using the Motorola process, though not significantly different from the results obtained with the unsintered plates using nickel only. Sintering obviously produced a dramatic improvement.

Table 17

Tab Pull Tests

Process	Tab Pull Strength (g)	
	Range	Mean (Std. Dev.)
Motorola	0-184	67 (59)
Brenner Nickel	0-249	98(106)
Halma Nickel	0-289	111(107)
Brenner Ni (sintered)	150-737	407(198)
Halma Ni (sintered)	113-601	319(161)

We have previously observed that sintering can create a major improvement in adhesion in some cases where adhesion is not very good prior to sintering. We have also observed that excellent adhesion is sometimes obtained without sintering. With these facts in mind we repeated the experiment of Table 17, but using only the Motorola process and the Brenner electroless nickel plating solution. Results are shown in Table 18.

Table 18

Tab Pull Tests

Process	Tab Pull Strength (g)	
	Range	Mean (Std. Dev.)
Motorola	62-400	288 (190)
Brenner Ni (unsintered)	57-451	248 (137)

It is evident that better adhesion was obtained this time in both cases, despite the fact that no conscious changes were made in the processing, and it is most significant that the Motorola process was affected in exactly the same way as was the simple electroless nickel plating process.

The Motorola process calls for five minutes of electroless nickel plating at 80°C, and these are the conditions we used in all of these experiments. We have previously reported (6) obtaining best results when plating for six to ten minutes at 90°C. Therefore, we believe that the relatively poor adhesion and great variability in the data of these experiments results from a nickel thickness which is somewhat less than ideal.

6.5 DIODES

Diodes were fabricated using both the Motorola process and the electroless nickel plating step alone, and diode quality factors (n factors) were determined from measurements of dark current as a function of bias voltage.

We know that these n factors (at the maximum power point) are near unity for our titanium/palladium/silver metallization but are usually closer to two for nickel/solder metallization, so we thought that any signficant differences between the products of the complex Motorola process and simple electroless nickel plating might be evidenced by a significant difference in this factor.

In our first experiment, effective diode n factors at 0.45 volt were found to be greater than two in all cases, and there was considerable scatter in the data, especially great in the Motorola process diodes. Some of the diodes made with the Motorola process showed n factors much greater than two, and removal of the metallization followed by measurements of sheet resistivity showed that the diffused region had been substantially altered. Consequently, this experiment was repeated using a deeper diffusion.

Reproducibility was much better in this second experiment, and results of the measurements are shown in Table 19. Dark reverse currents were subtracted from the dark forward currents in obtaining these n factors, and, in calculating average values, one diode was dropped from each group as being obviously shorted (forward and reverse currents nearly identical), and three diodes were eliminated (one from the Motorola process group and two from the nickel only group) because their n factors were more than three standard deviations higher than the means of their respective groups.

Table 19

Diode n Factors

Process	n Factor	Std. Dev.
Motorola (21 diodes)	2.29	0.24
Nickel Only (16 diodes)	2.21	0.26

Obviously these diode characteristics provide no distinction between the two metallization processes.

6.6 PHOTOVOLTAIC CELLS

Attempts were made to fabricate solar cells using the Motorola process with a variety of masking techniques to form the front metallization pattern. Screen printed inks, evaporated coatings and photolith processes, with and without baking or sintering treatments, were tried with little success. One or more of the various cleaning and plating solutions attacked the masking material in every case.

We did not attempt to use the silicon nitride of Motorola because 1) Motorola did not specify the details of their masking process, perhaps regarding the process to be a proprietary one, and 2) we have more experience with other materials.

We did achieve success using a relatively thick mask of silicon dioxide. We have shown previously (6) that the electroless plating solutions dissolve silicon dioxide, but the process is not a rapid one, and an oxide thickness of about 2,000 Angstroms appears to serve our purpose well.

In the first successful cell fabrication, round Cz wafers (2.94" diameter, p type) were used with phosphorus diffusion to form the p-n junction and with alloyed aluminum backs. About 1,800 Angstroms of SiO_2 was formed on the

fronts of the cells (Silox process), and a masking pattern was produced by photolithography and a buffered HF etch. The photoresist was removed in acetone prior to plating.

The pattern chosen had relatively wide metallized areas with large separations, and metal covered about 15% of the front cell surface. This is not a pattern calculated to produce efficient cells, but it was considered to be a desirable one for the purpose of comparing the two different metal plating procedures without introducing unnecessary complications or uncertainties related to the mask.

Eleven cells were fabricated using the Motorola sequence and thirteen cells were made using just the electroless nickel plating step of the Motorola process. We felt that the 1,800 Angstroms of SiO_2 might not be adequate to withstand all of the HF treatments of the Motorola process, so in this experiment we modified the process by reducing the HF treatments. We also felt that the HF treatments were probably not necessary, since SiO_2 is removed by the plating solutions, and, in fact, we observed no plating difficulties.

Illuminated I-V measurements were made on these cells at AM1, and the data are shown in Table 20. The thick SiO_2 coating was left in place for these measurements.

Table 20

Electrical Characteristics of Cells

Process		V_{oc} mV	I_{sc} mA	P_m mW
Modified Motorola (8 cells)	mean (std. dev.)	562.5 (13.1)	1048 (75)	363 (24)
Nickel Only (12 cells)	mean (std. dev.)	592.8 (5.9)	1058 (42)	370 (33)

There is little difference between the two groups in short circuit current and maximum power, the Motorola process group showing slightly lower values in each case, but cells made with the Motorola process show an open circuit voltage about 30 mV below that of the cells using nickel only. We believe this difference results from greater penetration of the diffusion layer by the Motorola process.

Three cells in the Motorola process group and one cell in the nickel only group were not included in the measurements of Table 20, because their metallization showed some obvious weakness. We suggest that this results from the relatively thin nickel plate obtained by plating for five minutes at 80°C, as discussed earlier in this report.

This experiment was repeated using a thicker SiO_2 mask (about 2,200 Angstroms) in combination with the complete

Motorola process. The wafers in this case measured 7.50 cm in diameter and the SiO_2 was removed and replaced with a tantalum oxide AR coating before measuring the electrical characteristics. Otherwise the processing was identical to that of the earlier experiment. Illuminated I-V data at AM0 from these cells are shown in Table 21. Four obviously inferior Motorola process cells were not included in these averages, two having very open circuit voltages, one having an exceptionally low short circuit current, and one showing abnormally low maximum power.

Table 21

Electrical Characteristics of Cells

Process		V_{oc} mV	I_{sc} mA	P_m mW
Motorola (13 cells)	Mean (std. dev.)	543.7 (6.4)	1370 (78)	445 (59)
Nickel (18 cells)	Mean (std. dev.)	550.6 (10.7)	1337 (39)	472 (24)

There is some scatter in these data, especially in short circuit current and maximum power, with the scatter being obviously greater in the Motorola process group, but again the data provide no other basis for choosing between the two processes.

6.7 BACK SURFACE METALLIZATION

Work has been concerned primarily with the quality of front surface metallization of solar cells, because metallization of back p+ surfaces, owing to its much greater area, normally causes fewer problems even when its quality is not very good.

Good back surface metallization has been obtained when using the Motorola process as well as when using electroless nickel alone. We have noted, however, that back surface solder is sometimes obviously rougher, with some gaps, on Motorola process specimens than on specimens plated with nickel only.

This is a subjective judgement, and frequently no distinction is evident, but it appears that, when a difference is obvious, the Motorola process specimens have poorer quality solder coatings on their backs.

7. CONCLUSIONS

7.1 Plating on Silicon Dioxide

Silicon dioxide films on cells prior to metallization (using an alkaline hypophosphite electroless nickel plating solution) do not harm contact quality, beyond the effects of nickel thickness. The plating solution dissolves silicon dioxide before plating nickel. There can be problems related to surface conditions, but such problems are caused by other impurities, not by silicon dioxide.

7.2 Thermal Stress Tests

In the environmental stress tests, cells performed well for 1,000 hours at 85°C, 85% relative humidity, and 0.45 volt forward bias, but the temperature extremes of -65°C and +150°C were too severe for these cells.

Nickel/solder metallization on silicon did survive well for over 750 hours at 100°C and for 25 cycles of thermal shock from -40 to +100°C.

At least two different failure mechanisms were operating in these tests, as evidenced by the two different modes of failure prevailing with the different kinds of stresses.

This observation implies that at least some of these tests are not valid as accelerated predictors of lifetime behavior, because an accelerated life test procedure, to be valid, must not alter the failure mechanism.

7.3 Sintering

Sintering temperatures should be limited to a maximum of about 300°C, and at this temperature lengthy sintering is safe but not essential. In many cases excellent contact adhesion is obtained from simple electroless nickel plating with no sintering beyond a few seconds in molten solder.

7.4 Influence of Plating Solution on Cells

Variations in plating time from 4 to 14 minutes at 90°C do not affect cell quality, again excepting the effects related to nickel thickness. Nickel thickness affects the quality of the contact, and an intermediate nickel thickness is most desirable (estimated to be approximately 0.5 μm).

The plating solution has been shown to etch silicon before depositing nickel.

7.5 Motorola Process

The Motorola plating process is an extremely cumbersome and time consuming process. Its reliability and reproducibility are not as good as the reliability and reproducibility of simple electroless nickel plating. It is compatible with a very limited number of pattern masking techniques.

We also conclude, on the basis of parallel experiments (adhesion measurements, diode characteristics and illuminated I-V characteristics), that the product of the Motorola process is essentially identical to the product of the single step electroless nickel plating process, with the exception that the Motorola process yields somewhat poorer reproducibility and demands better control of the phosphorus diffusion process.

8. RECOMMENDATIONS

No changes in process specifications for nickel plating can be recommended. Both the Motorola process and single step electroless nickel plating can produce good quality metallization on silicon solar cells. The two processes, though widely different, give virtually identical results, but the Motorola process is much too lengthy and complex to be used in mass production of low cost solar cells.

Cleanliness in process steps preceding nickel plating is more critical than any variations in the plating process itself. A variety of techniques may be used in processing prior to actual nickel plating, and these may cause contamination of the surface to be plated. There can be no single cleaning procedure guaranteed to remove all possible types of contamination, so process steps must be designed to maximize cleanliness and cleaning procedures should be developed which are effective and compatible with the processing techniques which are used.

Adhesion of metallization to silicon is dependent on the thickness of the plated nickel. It is therefore recommended for large scale production of solar cells that the thickness of the nickel plate be monitored. The optimum nickel thickness is a function of the exact method used to

plate the nickel and also of the solder dipping technique used (the solder dissolves some nickel), so this optimum thickness should be determined on the production line itself.

9. References

(1) Metallization of Large Silicon Wafers with Palladium-Nickel-Solder Metallization System. Motorola, Inc., Dec. 1978. JPL Contract 954689.

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(5) N. Hedgecock, P. Tung, and M. Schlesinger, J. Electrochem. Soc., 122, 866 (1975).

(6) R. C. Petersen, DOE/JPL Contract No. 954854, Sixth Quarterly Report, April, 1980, Solarex Corporation.

APPENDIX A

TAB SOLDER PROCEDURE FOR ENVIRONMENTAL STRESS TESTS

Soldering to Bus:

1. Erase AR coating, using ordinary pencil eraser, from bus area to which tab will be soldered.

2. Place cell on a heat sink (e.g. Al slab, 1/4" thick).

3. Place a small amount of solder paste (about 1 cu mm) on bus area to be soldered (solder paste = SCM Corp. ESP-150).

4. Place tab (70 mil wide, 2 mil thick, about 2" long tin-plated soft copper) across bus at point to be soldered so that the end of the tab is aligned with the center of the bus.

5. Press tab to cell with tip of soldering iron (Hexacon Thermotrac Model 1002 with 1/16" chisel tip - regulated at 600°F). Use quick strokes to avoid heating the cell excessively. Wipe soldering iron tip on a damp sponge prior to each application.

6. Place tabbed cells in an ultrasonic bath containing flux cleaner (Alpha Metals, Inc., #564) for five minutes, then rinse for five minutes in clean iso-propyl alcohol, and finally air dry.

Soldering to Back:

Follow the above procedure with the following modifications: step 1 can be eliminated; in step 3 add a little solder paste to the end of the tab; for step 4 place the end of the tab near the center of the back; in step 5 use a 1/8" chisel tip at 650°F and make the length of the bond approximately equal to the width of the chisel tip.

APPENDIX B

MOTOROLA PROCESS

A. INTRODUCTION

In pursuance of JPL Contract No. 954689, an advanced process for silicon solar cell metallization has been developed and demonstrated to be capable of permitting high reliability, large volume, and low cost. This metallization process, which has been demonstrated on a developmental laboratory scale, is specified in this document.

This process is the forerunner of a production-ready process and requires advanced development in order to be entirely suitable for the high through-put, low cost technology required for long term goals. For example, chemical plating solutions are now contained and used in small volume beakers rather than in large volume, continuously replenished tanks. Heat treatments are performed in quartz tube lined resistance heated furnaces rather than using a more appropriate belt furnace. The fundamental process has, however, been defined.

The process specified here is relatively complex and is considered to contain the maximum number of process steps required for assured metallization of n-on-p solar cells with n+ front surfaces and p+ back surfaces. It is possible that, in the future, this process may be altered or eliminated. To

date, attempts to shorten the process have met with varying degrees of success. Such attempts have been sufficiently successful to show feasibility, but not successful enough to guarantee a favorable outcome each and every time. This guarantee must be a prerequisite for a process sequence recommendation.

The process sequence recommended here may require minor modifications to account for different types of solar cell substrates and to account for the previous processing history of substrates prior to metallization. For example, while the initial rinse in a dilute hydrofluoric acid solution, as recommended here, is sufficient cleaning for most types of samples, some samples prepared in different fashion may require a more elaborate clean to ensure adequate plating to the silicon surface. The process does, however, assure a high quality metallization and cell performance on standard Motorola solar cells. Specific times, temperatures, weights and volumes have been given in the process specification. Unless otherwise stated, it has been found that minor variations in these quantities have little impact on process performance, thus ensuring that adequate process control will be feasible.

The metallization scheme is comprised of three layers. Palladium, through the formation of palladium silicide at elevated temperatures, forms the ohmic contact to the silicon surface. Palladium is deposited first with an immersion

palladium solution to a thickness near 50Å. Palladium thickness is increased with an electroless palladium plating solution to about 1000Å. Nickel, plated on top of the palladium silicide/palladium layer to a thickness of about 5000Å, forms a solderable interface. Lead-tin solder provides electrical conductivity and is applied by means of a dip in molten solder.

B. MATERIALS AND SUPPLY LIST

Wet Chemicals

Acetone

Ammonium fluoride, 40% NH_4F, semiconductor grade

Ammonium hydroxide (NH_4OH), 28% NH_3, semiconductor grade

Chlorothene V.G.

Deionized water (DI H_2O), 14 megohm-cm purity

Hydrochloric acid, 37% HCl, semiconductor grade

Hydrofluoric acid, 49% HF, semiconductor grade

Nitric acid, 70% NHO_3, semiconductor grade

Peanut oil

Solder flux, type RA, Kester No. 1544

Dry Chemicals

Ammonium chloride, NH_4Cl, reagent grade

Nickel chloride, $NiCl_2 \cdot 6H_2O$, reagent grade

Palladium chloride, $PdCl_2$

Sodium citrate, $Na_3C_6H_5O_7 \cdot 2H_2O$, reagent grade

Sodium hypophosphite, $NaH_2PO_2 \cdot H_2O$, reagent grade

Tin-Lead solder, Kester 60 Sn - 40 Pb

C. CHEMICAL SOLUTION PREPARATION

CAUTION! Chemcial exhaust hoods are required for safe preparation and use of chemical solutions.

Dilute Hydrofluoric Acid (50:1 H_2O:HF)

For approximately 3 liters of dilute HF solution add 60 ml HF to 3000 ml deionized water (DI H_2O). Stir to mix thoroughly. For use during processing solar cells, a 4 l teflon beaker is a convenient container. The container should be covered when not in use.

Immersion Palladium

The palladium chloride is most readily entered into solution when the solution temperature is elevated. Mixing is most easily accomplished using a Pyrex beaker (4 l) on a hot plate with a magnetic stirrer.

a) Heat 3000 ml of DI H_2O to approximately 40°C.

b) Add 9 ml of hydrochloric acid and mix.

c) Add 0.08 g of palladium chloride and dissolve thoroughly.

d) Add 200 ml of ammonium fluoride and stir until clear.

Allow this solution to stand a minimum of 4 hours before use and allow to cool to room temperature.

Aqua Regia (metal etch solution)

For 4 liters of aqua regia add 1 l of nitric acid to 3 l of hydrochloric acid mix thoroughly. Allow to stand until

activated as indicated by evolution of bubbles within the solution.

Palladium Stock Solution

Because palladium chloride is somewhat difficult to dissolve, it is convenient to prepare a concentrated stock solution which is diluted for use in electroless palladium bath. A beaker of at least 2 l capacity and a hotplate with a magnetic stirrer are convenient.

a) Heat 950 ml of DI H_2O to approximately 40°C.

b) Add 50 ml of hydrochloric acid and mix thoroughly.

c) Add 25 g of palladium chloride and stir until completely dissolved. This may require as long as 4 hours.

Electroless Palladium

This formula is for approximately 4 l of electroless palladium solution. A quartz or Pyrex beaker of about 7 l capacity is a convenient container and a hot plate with a magnetic stirrer is useful.

a) Add 320 ml of palladium stock solution to 640 ml of ammonium hydroxide. Allow to stand a minimum of 2 hours. It is recommended that the solution be stored overnight in a high density polyethelene bottle, or the equivalent.

b) Filter the solution, add to 3000 ml of DI H_2O and mix thoroughly.

c) Add 108 g of ammonium chloride and mix.

c) Add 15 g of sodium hypophosphite and mix.

Heat solution to 50°C for use and keep beaker covered to reduce evaporation. Maintain a pH near 9.7 by addition of ammonium hydroxide as needed.

Electroless Nickel

This formula is for approximately 4 l of electroless nickel solution. A quartz or Pyrex beaker of about 7 l capacity is a convenient container and a hot plate with a magnetic stirrer is useful.

a) Add 120 g of nickel chloride to 3500 ml of DI H_2O and mix thoroughly.

b) Add 200 g of ammonium chloride and mix.

c) Add 336 g of sodium citrate and mix.

c) Add 40 g of sodium hypophosphite and mix.

d) Add 500 ml of ammonium hydroxide.

Heat solution 80°C for use and keep beaker covered to reduce evaporation. Maintain a pH near 10 by addition of ammonium hydroxide as needed.

D. EQUIPMENT AND FACILITIES

a. CAUTION! Chemical exhaust hoods are required for safe preparation and use of acid solutions and plating solutions!

Either standard exhaust hoods or laminar flow exhaust hoods are suitable for mixing solutions and plating solar cells. Hoods should be equipped with running DI H_2O, acid drains, suitable work space, and temperature controlled, stirring hotplates. This, of course, assumes that this solar cell metallization process is to be practiced on a laboratory scale. Full production scale would necessitate a larger scale facility than beakers and hotplates.

b. For heat treatments a resistance heated, quartz lined furance tube, such as table-top style Thermco Mini-Brute, is recommended. Again, for large production it may be much more suitable to use a belt furnace arrangement.

c. Circular or square solar cell substrates can be dried (following plating and rinsing operations) satisfactorily by centrifigal spin dryers, such as the Fluoroware Model K100.

d. Circular solar cell substrates can be conveniently handled in batches of up to 25 cells by using standard teflon wafer carriers for wet chemistry steps and standard quartz boats for heat treatments. These teflon carriers and quartz boats are

compatible so that wafers may be dump transfered from one to the other.

e. In promoting good plating reactions at the silicon surface in the immersion palladium solution, it has been found that high ambient light levels are desirable. To achieve this, a high intensity lamp, such as the quartz-halogen projector lamp type ENH, is mounted approximately two feet above the beaker containing the immersion palladium solution.

f. Soldering of individual cells can be accomplished with a soldering system as simple as an ordinary solder pot which merely melts and contains the solder and controls the molten solder temperature. The dimensions of the pot must be large enough to permit vertical entry of a solar cell.

Equipment List

Teflon, Pyrex, or Quartz Beakers and Lids

Teflon Wafer Carriers

Water Rinse Tanks

Wafer Spin Dryer

Thermometers

Hi-Intensity Lamp, 120V, 250 Watts

Timers

Teflon Stirring Rods

Equipment List (con't)

Hot Plates, equipped with magnetic stirrers and temperature controls

Nalgene Storage Bottles -- 1000 ml and 1 gal.

Teflon Tipped Tongs

Teflon Tweezers

Exhausted hood with acid and solvent drains and running DI H_2O

Protective Gloves

Protective Clothing

Funnels

Polypro Graduated Beakers

Graduated Cylinders

Solder Dip Station

Sintering Furnace, Quartz lined, with N_2 flow

Quartz Furnace Wafer Carriers

E. PROCESS SEQUENCE AND PROCEDURES

Step 1. Immersion Palladium Coat

1.1 Load cells into teflon carrier.

1.2 Place loaded carrier into 50:1 H_2O:HF solution for 30 sec. Use gentle agitation.

1.3 Directly from 50:1, place carrier into immersion palladium solution.

1.4 Turn on high intensity light over immersion palladium solution. Agitate carrier continuously for 3 min.

1.5 Rinse carrier and cells for 5 min. in running DI H_2O.

1.6 Place carrier and cells into aqua regia for 5 sec.

1.7 Rinse wafers for 15 min. in running DI H_2O.

1.8 Place carrier into 50:1 solution for 20 sec. Use gentle agitation.

1.9 Directly from 50:1, place carrier into immersion palladium solution illuminated by high intensity light for 5 min. with continuous agitation.

1.10 Rinse carrier and cells for 5 min. in running DI H_2O and spin dry.

1.11 After drying, inspect cells for immersion palladium coverage. Plated silicon surface appearance should be hazy with a light tan color.

Step 2. Heat Treatment

2.1 Dump transfer cells from teflon carrier to quartz boat for furnace.

2.2 Place boat into center of furnace hot zone at 300°C for 15 min. Use a continuous nitrogen purge and an end cap on the quartz tube.

2.3 Remove boat with cells and allow to cool.

2.4 Dump transfer cells back into teflon carrier.

Step 3. Electroless Palladium Plate

3.1 Immerse carrier of cells into 50:1 solution for 20 sec. with agitation.

3.2 Directly from 50:1 solution, place carrier into immersion palladium solution illuminated by high intensity light for 2 min. with continuous agitation.

3.3 Rinse in running DI H_2O for 2 min.

3.4 Place carrier of cells into electroless palladium solution for 45 sec. using gentle agitation. Solution temperature should be 50°C and ambient light level should be very low.

3.5 Rinse cells for 10 min. in running DI H_2O and spin dry.

3.6 After drying, inspect cells for electroless palladium coverage. Plated silicon surface should have a bright metallic finish with a warm, gold coloration.

Step 4. Heat Treatment

4.1 Dump transfer cells from telfon carrier to quartz boat for furnace.

4.2 Place boat into center of furnace hot zone at 300°C for 30 min. Use a continuous nitrogen purge and an end cap on the quartz tube.

4.3 Remove boat with cells and allow to cool.

4.4 Dump transfer cells back into teflon carrier.

Step 5. Electroless Nickel Plate

5.1 Immerse carrier of cells into electroless nickel solution for 5 min. using gentle agitation. Solution temperature should be 80°C.

5.2 Rinse cells for 10 min. in running DI H_2O and spin dry.

5.3 After drying, inspect cells for electroless nickel coverage. Plating should have very bright, metallic appearance.

Step 6. Solder

In the process described in this step, each cell is individually solder coated and given an initial solvent rinse. When a teflon carrier full of cells (one batch) is accumulated, all cells are given a final rinse and dry.

6.1 Load cell into teflon tipped soldering tongs.

6.2 Using tongs, immerse cell into soldering flux, then allow excess flux to drain.

6.3 Using tongs, immerse cell into solder pot at 240°C for approximately 1 sec. The surface of the solder pot is covered with peanut oil to prevent dross formation on the molten solder surface.

6.4 Allow cell to cool and solder to solidify in horizontal position.

6.5 Immerse cell into a beaker of chlorothene and agitate to remove most flux residue and oil.

6.6 Place cell into teflon carrier which is immersed in a second beaker of chlorothene. Let stand until carrier is full or each cell in lot has been soldered.

6.7 When carrier is full or soldering is complete, agitate carrier in chlorothene then place in beaker of acetone. Let stand for 5 min.

6.8 Rinse cells in running DI H_2O and spin dry.

APPENDIX C

SOLAREX PLATING PROCESS

Where 'Solarex plating process' or 'Solarex process' is used in this report, it refers to a specific plating process included as part of a cell fabrication process developed by Solarex under JPL contract number 954854 and described in a process specification submitted to JPL entitled "Material, Supply and Process Specifications and Process Procedures for Phase 2 of the Array Automated Assembly Task". Relevant excerpts from this process specification are repeated here.

1. Negative Silk Screening Requirements

1.1 Materials

a. Resist Ink: Astro-Var Interior Polyurethane Varnish for Floors, Furniture, Woodwork and Doors.

Astro-Var Gloss, Linseed Oil Modified
Polyurethane Resin Type I..50%
Mineral Spirits............50%

Supplier: Martin-Senour Company
Cleveland, Ohio 44113

b. Resist Thickener: Titanic Oxide

Anhydrous

Code #T-315

TiO_2...F.W. 79.9

Fisher Scientific Company

Chemical Manufacturing Division

Fair Lawn, New Jersey 07410

Combine 96g of TiO_2 with 56g of Polyurethane until homogeneous.

c. Resist Remover: J-100

Use hot (90 - 100°C)

Indust-Ri-Chem Laboratory (IRCL)

726-32 South Sherman Street

Richardson, Texas 75080

d. Screen Cleaner: NAZ-DAR

No. 2555

Screen Wash (XYLOL)

NAZ-DAR Company

Chicago, Illinois 60622

1.2 Equipment

a. Silk Screen: Polyester Monofilament Screen

Mesh size: 200 square per inch

Screen size: 10" x 12"

b. Stencil: Polyvinyl Acetate Emulsion

Pattern size: 0.122" for central bus bar

0.025" for finger

22 parallel fingers spaced 3/16" apart

c. Squeegee: Vinyl

Size: 1" L x 0.25" W

with 90° edges

Supplier (a,b,c): Prestige Screen Printing

14674 G. Southlawn Avenue

Rockville, MD 20850

d. Exhaust Hood

2. Electroless Nickel Plating Requirements

2.1 Materials

a. Plating Solution: Electroless Nickel Plating

Solution 139-500011-71

	Supplier:	J. E. Halma Co., Inc.
		91 Dell Glen Avenue
		Lodi, New Jersey 07644
b.	Ammonium Hydroxide:	B & A
		Ammonium Hydroxide
		Reagent A.C.S.
		Meets A.C.S. Specifications
		Code AX-1303
		Code 124-5760
	Supplier:	Allied Chemical Corporation
		Specialty Chemical Division
		Morristown, New Jersey 07960
c.	Acetone:	Technical Grade
		Stock #1005
	Supplier:	North Strong
		7322 Westmore Road
		Rockville, MD 20850
d.	Hydrofluoric Acid:	Technical Code HX 622
		52%
		Code #194-1102

Dissolve 20 parts water to 1 part HF.

Supplier:	Allied Chemical Corporation Morristown, New Jersey 07960

2.2 Equipment

a.	Nickel Plating Tank:	Polyvinylchloride, constructed in-house
	Dimensions:	8 inches deep x 8 inches wide x 14 inches long
	Supplier:	Read Plastics 12331 Wilkins Avenue Rockville, MD 20850
b.	Nickel Plating Tank Heater:	Quartz covered electric resistance heater, 2 each, 1 KW each
	Dimensions:	.5 inch diameter, 12 inches long
	Supplier:	Chemical Etching Equipment & Supply 7629 Crawford Court Alexandria, VA 22310
c.	Nickel Plating Tank Pump:	Rotary circulating pump Little Giant #2 MD
	Supplier:	Virginia Pump Company 1743 King Street Alexandria, VA 22314

d.	Rinse Station:	Fabricated Cascade Rinse Tank
		Part #E62
	Dimensions (mm):	190L x 171.4W x 114H x 660 over-all length
	Supplier:	Fluoroware
		Jonathan Industrial Center
		Chaska, MN 55318
e.	Cassettes:	Plastic Wafer Holder
		100 mm wafer capability
		Part # A72-40M
	Dimensions (mm):	142.2L x 127W x 114.3H
	Supplier:	Fluoroware
		Jonathan Industrial Center
		Chaska, MN 55318
f.	Hydrofluoric Acid Bath:	Polypropylene
		Molded Round Tank
		E14 Series
		PE14-100-01 tank
		PE14-100-02 cover
	Capacity:	10,000 ml
	Diameter:	10.5" depth: 8"
	Supplier:	Fluoroware
		Jonathan Industrial Center
		Chaska, MN 55318

g. Spin Dryer: Rinser-Dryer
Model K-13C with Model 501
Console for 4" wafers
0-10,000 rpm

Dimensions (cm): 66L x 66W x 86H

Supplier: Fluoroware Systems Corporation
335 Lake Hazeltime Drive
Chaska, MN 55318

3. Process Specification

3.1 Negative Silk Screening

Operator safety requires that silk screening and screen cleaning be conducted under an exhaust hood. Safety precautions for flammable solvents must be observed.

The silk screen is designed to print a masking ink on those areas of the wafer which are not be be electroless nickel plated. The wafer is aligned beneath the screen and printed. Screen offset is 1/8 inch, angle is 45°, pressure is 40 lbs., single stroke. These figures are approximate for hand silk screening. The screening operation can run continuously until the quality of reproduction becomes unacceptable as evidenced by poor line edge acuity, or inadequate transmission of ink. Approximately 1000 cycles can be expected before screen cleaning or replacement is required.

Xylol is the solvent used for screen cleaning and general cleanup. After printing, the wafers are dried under heat lamps placed 4 inches above the cells for three minutes (± 15 sec.). Temperature is 160°C ± 5°C.

3.2 Electroless Nickel Plating

Nickel plating must be carried out under an exhaust hood. Operator safetv requires use of safety glasses, gloves, and apron.

The silk screened wafers are loaded into teflon cassettes and etched in 20:1 HF at room temperature for 5 seconds. Rinse is in a tap water cascade for 10 minutes. One liter of water per wafer is required.

The nickel plating solution is heated to 90°C (+5°C, -0°C) and a pH is maintained at 8.2 by carefully adding ammonium hydroxide when necessary. The rate of addition must be slow to avoid a hazardous reaction. The wafers are then immersed in the plating solution for 6 minutes. The wafers are rinsed in tap water for approximately 5 minutes. The resist ink is removed by immersing the cells in boiling IRCL resist remover for about 3 minutes until clean. The cells are then rinsed in tap water (17°C - 4[illegible]°C) for 15 minutes and spun dry at 500 rpm for 120 seconds.